Design and Implementation of High Frequency and Low-Power Phase-locked Loop

Premananda B. S.[1], Dhanush T. N.[2], Vaishnavi S. Parashar[3], D. Aneesh Bharadwaj[4]

[1]Department of Electronics and Telecommunication Engineering, RV College of Engineering, Bengaluru, India (premanandabs@gmail.com) ORCID 0000-0001-7740-7659; [2]Department of Electronics and Telecommunication Engineering, RV College of Engineering, Bengaluru, India (dneel31051998@gmail.com); [3]Department of Electronics and Telecommunication Engineering, RV College of Engineering, Bengaluru, India (vaishnavisparashar@gmail.com); [4]Department of Electronics and Telecommunication Engineering, RV College of Engineering, Bengaluru, India (bharadwajaneesh390@gmail.com)

Abstract

Phase-locked loop (PLL) operates at a high frequency and due to the increased switching rate of the circuits, the power consumption is high. Designing a PLL which consumes less power without compromising the frequency of operation is essential. The sub-components of PLL such as the phase frequency detector, charge pump, loop filter, voltage-controlled oscillator, and the frequency divider have to be designed for reduced power consumption. The proposed PLL along with its sub-components have been designed using the CMOS 180nm technology library in the Cadence Virtuoso and simulated using Cadence Spectre with a supply voltage of 1.8V resulting in a 20% reduction in power with a higher frequency of operation compared to the reference PLL architecture. The capture range and lock range of the proposed PLL are 2.09 to 2.14 GHz and 1 to 3.5GHz, respectively. The designed PLL consumes less power and operates at a higher frequency.

Author Keywords. Charge Pump, CMOS, CSVCO, PFD, PLL, VCO.

Type: Review Article

1. Introduction

A communication system with low power consumption, higher performance and reduced jitter is considered highly efficient. A Phase-locked loop (PLL) can track an input frequency, synchronize signals and generate a frequency that is a multiple of the input frequency (Kaipu et al. 2016; Ravisaheb and Nagpara 2017). The system-level block diagram of a PLL is shown in Figure 1. The components- Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), Voltage Controlled Oscillator (VCO) and the frequency divider (Divide by N counter) are integrated to form the mainframe of the PLL system. The phase difference that exists between the two input signals is proportional to the output produced by the PFD. A minimum phase error can be achieved by producing a DC voltage that controls the VCO. The charge pump circuit is used to combine the two outputs of the PFD into a single output, which is then fed into the input of the loop filter (Praseetha, Benedict Tephila, and Anusuya 2019).

The components of the PLL consume a certain amount of power. When integrated using the existing architectures, components are found to consume more power that increases further as the frequency of operation increases. To address this problem, each component has to be selectively implemented using techniques such as reduction in the number of transistors, sizing of the transistors, and the connection of the bulk. After selectively reducing the power

of the individual components, each of these components should be integrated together to obtain a better power efficiency. The need for a low-power circuit that operates at a higher frequency is a major requirement of the PLL. PLL, being a major component in the communication systems, has a VCO that is active for a larger part of the operating time. The VCO has a higher switching rate resulting in higher power dissipation of the PLL system. There is a need to design a PLL system with reduced power consumption.
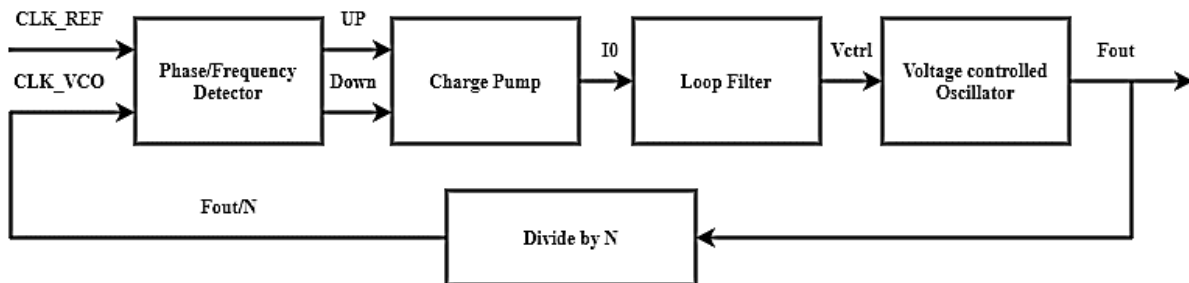

Figure 1: General block diagram of the PLL

The individual blocks of the PLL, such as PFD, charge pumps, loop filter, VCO, and frequency divider, are implemented with the goal of reducing the power consumption. These blocks subsequently are integrated to form a low-power PLL. The objective of this study is not only to reduce power consumption but also to increase the frequency of operation of the PLL. The PLL designed in this study fulfils both.

The organization of the paper is as follows; section 2 discusses the literature review of various architectures of sub-components of the PLL, section 3 discusses the components of the PLL. Obtained results are further discussed in section 4. Conclusions derived from the study are covered in section 5.

2. Related Works

A PLL is one of the essential parts of the transceiver circuit. The major application of the PLL circuit is to provide a stable clock. A conventional Integer-N PLL based frequency synthesizer, an application of PLL is mentioned in Kaipu et al. (2016). A PLL of order three with low power, fully integrated with a wide range of operation has been discussed in this paper. The design is also used in the ZigBee applications and is operated for a control voltage range of 1.4 to 1.8 V at a frequency of 2 GHz. Provision of clocking schemes in any electronic circuit is essential and is fulfilled by the implementation of the PLL circuit (Ravisaheb and Nagpara 2017). PLLs' should consume low power as the usage of a PLL in the circuits, which constitute its application, is bound to consume an exceptionally high power.

A wide range frequency satisfying PLL for GSM applications is mentioned in Nanda, Acharya, and Patra (2013). The PLL mentioned here is used for wireless communication to correct the errors in the phase and frequency in the GHz range with synchronization being provided for a lower locking time and reduced skew-time and jitter. The concept of designing a PLL for low lock in time and high capture range has been mentioned.

To enable a reduction in the number of transistors and thereby reducing the power consumption of the VCO, the pseudo NMOS based VCO has been proposed in Das et al. (2018). This proves helpful while considering designing low power consumption PLL. A divider less PLL with low power and jitter is presented in Ghaderi, Erfani-jazi, and Mohseni-Mirabadi (2016). A PFD with reduced power consumption is proposed. A Wilson charge pump circuit, which has an enhanced performance because of optimized algorithms to get a high output swing and matching of the current, is also proposed. The PLL is designed using 180nm CMOS technology

with a 1.8 V power supply. In addition to these parameters, a dead zone free PFD is also mentioned.

A PLL with a current starved voltage-controlled oscillator (CSVCO) in 180nm CMOS technology is mentioned in Sen and Jain (2014). For a reference frequency of 50 MHz, the CSVCO has an output frequency of 1 to 3 GHz at a supply voltage of 1 V. The applications of PLL such as clock generation and recovery is mentioned. Application of PLL and types of PLL are discussed in (Nargund et al. 2016). PFD with Dead zone is used in the design of low power PLL (Bency et al. 2021). MOSFETs are used for the design of loop filter. Adaptive voltage level (AVLS) technique is incorporated in the circuit to reduce power consumption of the PLL.

The proposed work aims at re-sizing the transistors to increase the frequency of operation, as well as decrease the power consumption.

3. Theory and Fundamentals of a Phase-Locked Loop

The PLL is a control system that compares the phase of the feedback signal with the phase of the input signal. The PLL and its subcomponents are discussed in this section. A PLL is a system that consists of interconnected components and it has a negative feedback configuration. The components of PLL are designed to operate at a higher frequency (GHz).

3.1. Phase frequency detector

Phase detector (PD), is a logic circuit used to generate a voltage signal representing a phase difference between the two input signals. A PD can be XOR or PFD based. PFD compares only the rising edges of the two input signals, and thus the width of the input signal is insignificant. PFDs are implemented using D flip-flops. In order to reduce the clock skew problem, TSPC based flops are recommended to implement PFD. When the phase difference between the two input signals is close to zero, the width of the output signal produced by the PFD will be very small. The low width UP and DOWN signal will not be able to charge and discharge the switches of the charge pump and thus cannot produce an output which can be given to the LF to produce a constant DC control voltage to the VCO.

The phase difference between the two input signals CLK_REF and CLK_VCO are indicated in the equation (1). The phase error $\Delta\emptyset$ is zero when the PLL is in a locked condition.

$$\Delta\emptyset = \frac{\Delta t}{Tref} \tag{1}$$

where, $\Delta\emptyset$ = Phase error

Δt = Time delay between the peak of two input signals

$Tref$ = Time period of the input reference signal

The output voltage of the PFD, VPFD, calculated using the equation (2).

$$VPFD = \left[\frac{VDD - 0}{4\pi}\right] \cdot [\Delta\emptyset] \tag{2}$$

Thus, the gain of the PFD is calculated using the equation (3).

$$KPFD = \frac{VDD}{4\pi} \tag{3}$$

where, KPFD = Gain of the PFD (volts/rad)

3.2. Charge pump and loop filter

The charge pump circuit combines two outputs of the PFD into a single output, which is further fed as an input to the loop filter. The charge pump consists of a current source, two latches for two signals UP and DOWN that are outputs of the PFD. When the UP signal is high, the current flows into the circuit. When the DOWN signal is high, the current flows out of the circuit. The second order loop filter consists of a resistor in series with a capacitor that is

parallel to a capacitor. The resistors and capacitors designed are set at the required values for frequencies using the basic second order low pass filter design given in the equation (4).

$$f = \frac{1}{2\pi R1 (C1 \cdot C2)^{0.5}}$$

(4)

Using equation (4) the resistance and capacitances are calculated and used in designing the loop filter. The loop filter used in the PLL circuit provides two functions. One is stability and the other is to reduce the ripples from the PFD output, which is applied to the VCO.

3.3. Voltage controlled oscillator

A VCO is an oscillator that takes the control voltage as an input and produces a sinusoidal or a square wave as an output depending on the type of oscillator used. Two architectures of VCOs are considered for the implementation: the current starved VCO (CSVCO) and pseudo NMOS based VCO. In a CSVCO, the output of the last inverter is given as a feedback to the first inverter, and the oscillations that begin initially are carried forward by the stages of inverters. CSVCO is a combination of the chain of an odd number of stages of inverters along with the current mirror circuit and the transistors, which act as a current source present above and below each stage of the inverters. The proposed VCO is based on the five-stage CSVCO (N = 5). The VCO is found to have lower power consumption and less area (transistor count).

3.3.1. Design of the voltage controlled oscillator

The five-stage CSVCO is designed with the center frequency of VCO at 2.08 GHz. For a VCO to work in its tuning range (i.e., from minimum to maximum frequency), the minimum frequency occurs at any value of the control voltage above the threshold of the NMOS for which the input of the control voltage is given. The maximum frequency occurs when the value of the control voltage is equal to the supply voltage. The threshold voltage of the NMOS transistor is found to be 0.548 V, which yields a minimum frequency of 647 MHz. The VCO when applied with a control voltage of 1.8 V yields a maximum frequency of 2.425 GHz. The center frequency is designed to be 2.08 GHz at a voltage of 0.9 V where the width of both PMOS and NMOS transistors is sized to 1 µm.

The calculations are done according to the values of the transistor sizing, capacitance, supply voltage, center frequency, current, and number of stages of the CSVCO. The calculation of the oscillating frequency of the VCO (F_{osc}) is achieved using several parameters including the supply voltage; total capacitance of the MOSFET and others is discussed in this section. The oscillating frequency equation is arrived at using the average current equation. The average current is assumed to be equal to the drain current, given by

$$I_{avg} = \frac{N \cdot \left(\frac{V_{dd}}{2}\right) \cdot c_{tot}}{(T)}$$

(5)

I_{avg} is the average current, N is the number of stages in a VCO, the supply voltage is V_{dd} (1.8 V) and total capacitance of the MOSFET is c_{tot}. The time period is inverse to that of the oscillating frequency (F_{osc}), the equation (6) can be redefined to find F_{osc}.

$$F_{osc} = \frac{Id}{(N \left(\frac{Vdd}{2}\right) c_{tot})}$$

(6)

The total capacitance of the MOSFET is one of the essential parameters required for the calculation of the oscillating frequency and is obtained using the equation (7).

$$c_{tot} = \left(\frac{5}{2}\right) \cdot c_{ox} \cdot (W_p L_p + W_n L_n)$$

(7)

The calculation of c_{tot} requires predefined values such as the widths and lengths of PMOS and NMOS and the oxide capacitances (c_{ox}). The oxide capacitance is given by

$$c_{ox} = \frac{\varepsilon_0 \cdot \varepsilon_r}{T_{ox}}$$

(8)

The VCO is designed using 180nm CMOS technology. The predefined values of all the required parameters in the equation (8) are considered and the value of c_{ox} is calculated. For CMOS 180 nm technology, the permittivity of free space is $\varepsilon_0 = 8.85 \times 10^{-18}$ F/μm^2, relative permittivity of the MOSFET is found to be 3.97 and the thickness of the oxide is 4×10^{-9}. The value of oxide capacitance is 8.784 fF/μm^2. These values are substituted in the equation (8) to calculate the total capacitance of the MOSFET. The resulting total capacitance is 7.9056fF. Considering the total capacitance of the MOSFET, with the supply voltage of 1.8V, the drain current to be 73.5 μA, the resulting oscillating frequency is found to be 2.08 GHz as desired.

3.4. Frequency divider

The frequency divider circuit is present in the feedback path of the PLL. The longer interconnects and high capacitive loading result in longer transitions and clock skew problems. The clock skew problem will limit the operating speed of the system. To reduce the clock skew problem, True Single-Phase Clock (TSPC) logic is suggested (Anirvinnan et al. 2019). TSPC is a clocking scheme wherein the clock used in the circuit is never inverted. TPSC logic results in higher performance of the system by eliminating the clock skew problem, performing at higher frequency and occupying lesser area. These circuits also have lesser phase noise.

4. Design and Implementation of Low-Power Phase-locked Loop

The PLL is designed and implemented using Cadence Virtuoso in CMOS 180nm technology and is simulated using Cadence Spectre. The implementation is done in the bottom-up approach where the components of PLL such as the PFD, CP, LF, VCO and divide –by-2 counters are first designed and then integrated to obtain the required PLL circuit. The design and implementation of the components along with the integration of the PLL is discussed in this section.

4.1. Design and implementation of the proposed phase frequency detector

PFDs are always active resulting in high power consumption. There is a need to redesign PFDs in order to reduce the power consumption when integrating it in the PLL. A method is proposed to eliminate the reset path and to share the reference clock and VCO clock signal in the initial stages. Figure 2 depicts the block diagram of a PFD circuit based on which the architectures are implemented. The D input of the flip-flop is kept high and the clock signals fed to the D flip-flops are CLK_REF and CLK_VCO to the upper and lower flip-flops respectively. The outputs of these flip-flops are then given to the reset circuit. The reset path mentioned here may be any logic gate based on the requirements of the PFD circuit. The PFD can be MUX based, pass-transistor based (Ravisaheb and Nagpara 2017), TSPC based PFD (Praseetha, Benedict Tephila, and Anusuya 2019) or PFD without reset path (Thakore, Shah, and Devashrey 2019). The reset path is a feedback line followed back to the input line. The feedback or the reset path used in the circuit is the NOR gate. The NOR gate is fed with Up and Down outputs of the PFD and the resulting output is given as one of the inputs at the initial stages. The usage of this reset path may be cumbersome sometimes due to an increase in the usage of transistors which further increases the area consumed. The reset path is recommended to be replaced by sharing the reference clock and VCO clock signal in the initial stages (Das et al. 2018). This concept of replacing the reset path is carried out and a new design of PFD is proposed. The proposed PFD circuit without the reset path consists of 14

transistors. The PMOS and NMOS transistor count is 8 each. The Cadence Virtuoso implementation of the proposed PFD circuit without reset circuit is illustrated in Figure 3.
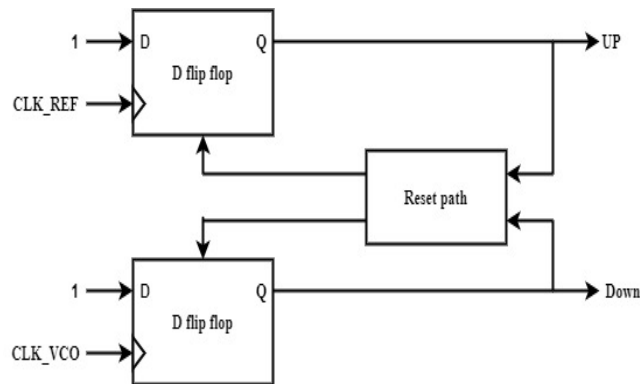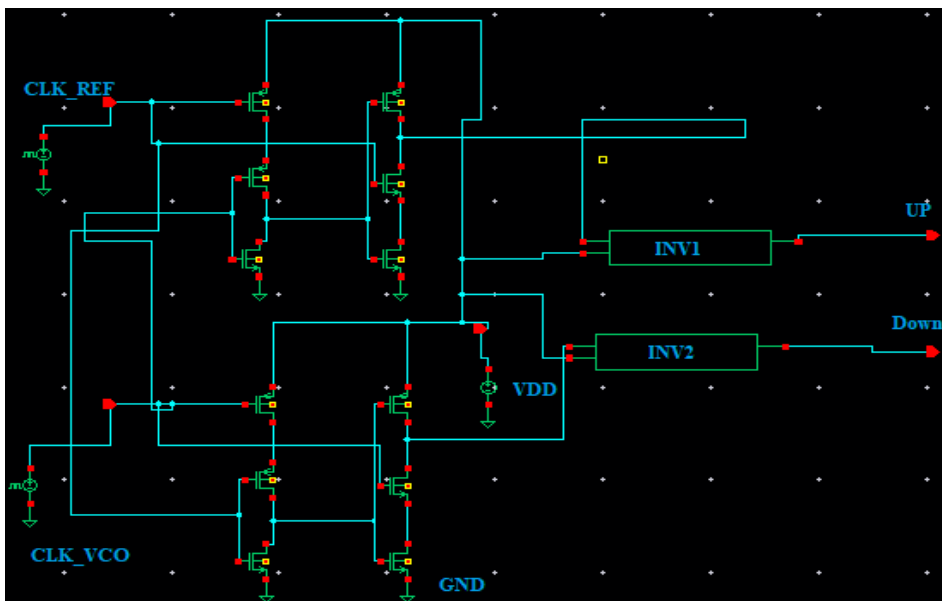

Figure 2: Block diagram of PFD

Figure 3: Proposed PFD circuit without reset

4.2. Design and implementation of charge pump and loop filter

A charge pump circuit consists of a current source and two inputs from PFD with latches to control the flow of current in and out of the filter. The filter, usually a low pass filter, is implemented and then integrated with the charge pump. The filter is designed based on the second order derivatives and the values of resistors and capacitances are calculated using this second order derivative. The implementation of the charge pump integrated along with the loop filter is shown in Figure 4. The outputs from the PFD are given to the charge pump circuit with the current source implementation in the circuit and the loop filter being integrated to the charge whose resistance and capacitances are calculated.
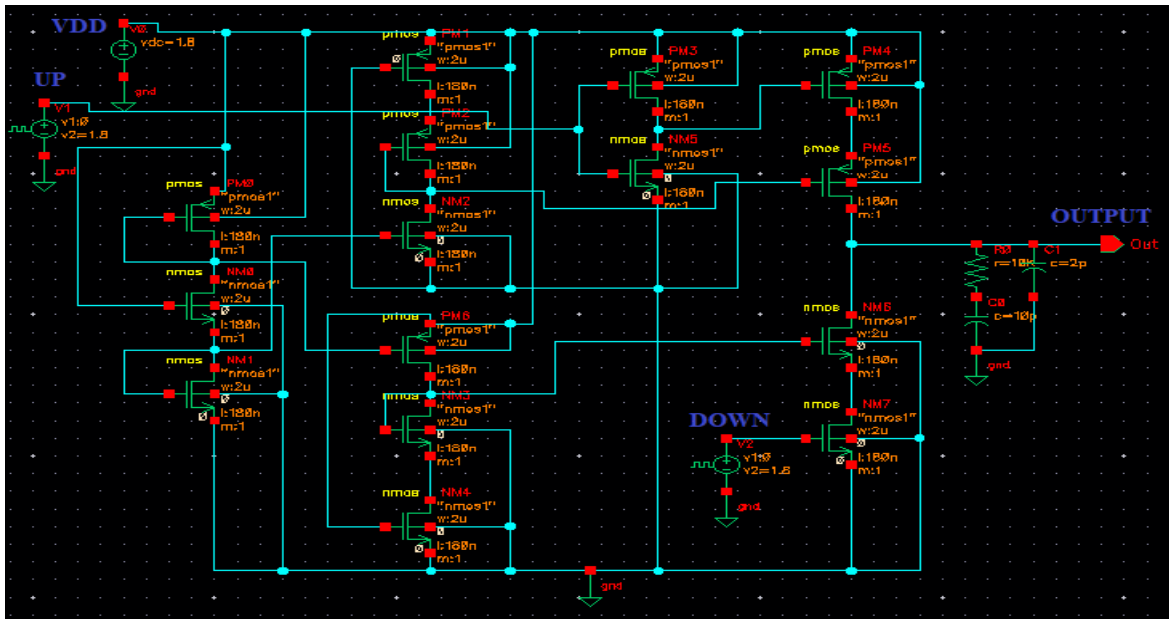
Figure 4: Circuit of charge pump integrated with a loop filter

4.3. Design and implementation of voltage controlled oscillator

The VCO is used to produce the sinusoidal output for the control voltage as an input. There is a linear increase in the output frequency of the VCO as the control voltage increases. The two types of VCOs that are used for the circuit implementation are CSVCO and the pseudo NMOS based VCO. In a CSVCO, the number of stages can be any odd number such as 3, 5, 7 and so on. The inverters whose numbers are equal to the stages of the VCO are cascaded and they have current sources in form of the transistors.

4.3.1. Five-stage current starved VCO

Cadence implementation of the five-stage CSVCO is indicated in Figure 5 with a supply voltage of 1.8 V. The left most transistors form a part of the current mirror circuit. The transistors form an inverter in the first stage and the subsequent transistors to the right of them form a part of the inverters which are in a cascade. The control voltage, the input to the VCO is given to the lower current mirror transistor. The transistors forming the current source form the critical part of the circuit. They ensure that only the necessary amount of current is provided to the inverters thereby "starving" them of the additional currents that can pass through them. The transistors of the inverters are sized according to the design mentioned. The numbers of stages being five, the inverters are cascaded, and the current mirror circuit along with the transistors acting as the current source can be seen. The output of the last stage is given as a feedback to the first stage. The control voltage, which is the input of the VCO, is varied from 0.6 to 1.8 V. The 0.6 V is the threshold voltage of the NMOS transistor to which the control voltage is connected. The operating frequency is varied from 647 MHz to 2.425 GHz where the center frequency of 2.08 GHz, which is the desired frequency, is achieved at a control voltage of 0.9 V which is exactly half the supply voltage. For a frequency beyond 2.425 GHz, as the control voltage increases, the output is not sinusoidal, and hence the maximum operational frequency is considered to be 2.425 GHz.
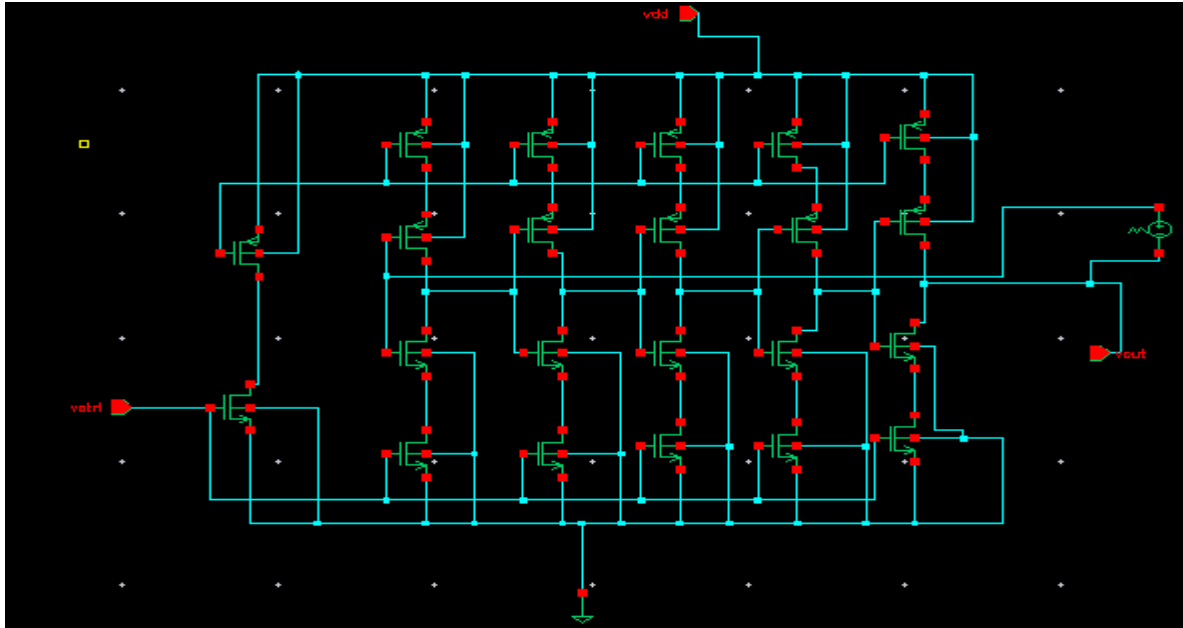
Figure 5: Circuit of the five-stage CSVCO

4.3.2. Pseudo NMOS based VCO

CSVCO when implemented using pseudo NMOS based logic is termed as a pseudo NMOS based VCO. The pseudo NMOS based VCO has a lesser number of transistors compared to CSVCO (Belorkar and Ladhake 2010). In the proposed design, five inverters are cascaded in order to produce oscillations. Since the number of transistors is reduced, the chip area also reduces. The proposed VCO is designed by sizing the NMOS and PMOS in order to achieve higher frequency of oscillations and to reduce the power consumption. In the five-stage CSVCO there are five PMOS that act as a current source. In the proposed design, instead of five PMOS transistors, a single PMOS transistor is used. In the current sinking circuit, conventionally, there are five NMOS transistors, but here a single NMOS transistor replaces them. Figure 6 shows the Cadence implementation of the pseudo NMOS based VCO.
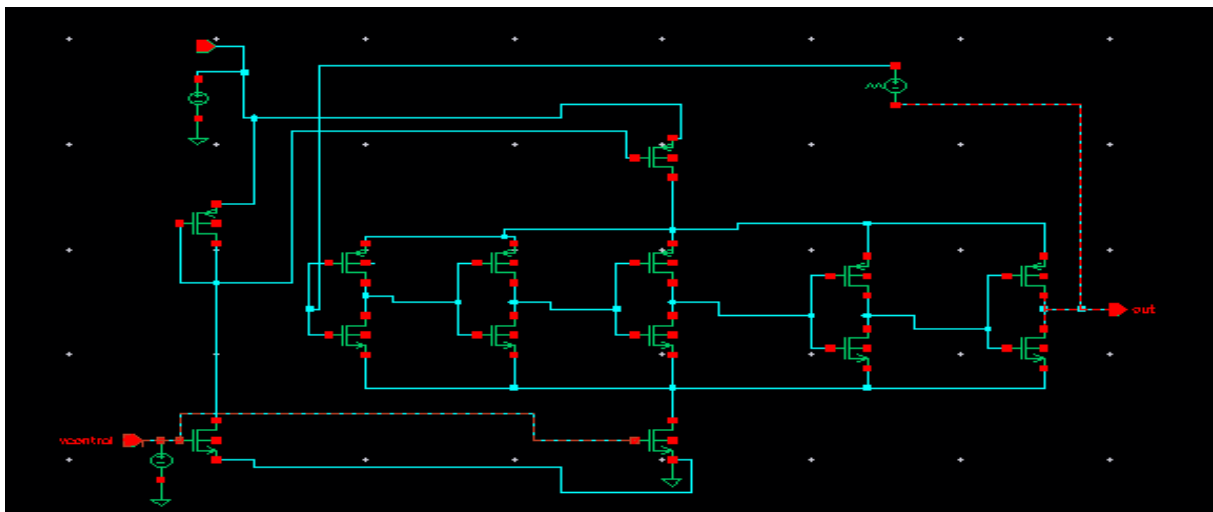

Figure 6: Proposed pseudo NMOS based VCO

The reference circuit is designed with the NMOS and PMOS width of 2μm. In the proposed VCO, the transistor resizing of the inverter is performed. Both NMOS and PMOS are sized with 1μm as their width. By performing the transistor resizing, the frequency range of oscillation is increased compared to both conventional CSVCO as well as Pseudo NMOS based VCO without sizing. The transistor count is reduced by eight when compared to that of CSVCO. Here only

one PMOS acts as the current source and there is only one NMOS which acts as current sink. The output of the last stage is given as a feedback to the first stage.

4.4. Design and implementation of the frequency divider

The frequency divider can be a simple divide by N counter or it can be a dual modulus N/N+1 pre-scaler. Figure 7 depicts the Cadence based schematic of a divide-by-2 counter that uses TPSC logic where the output is given to the input terminal D as a feedback. The 9T-TSPC based D Flip-flop is utilized in the implementation of the counter. Since TSPC logic is used for the implementation, the number of transistors is reduced and so is the phase noise of the circuit (Anirvinnan et al. 2019). The design is more compact and thus power consumption is less. The signal coming from the VCO is provided to the divide-by-2 counter; output of which is given as feedback to the PFD.
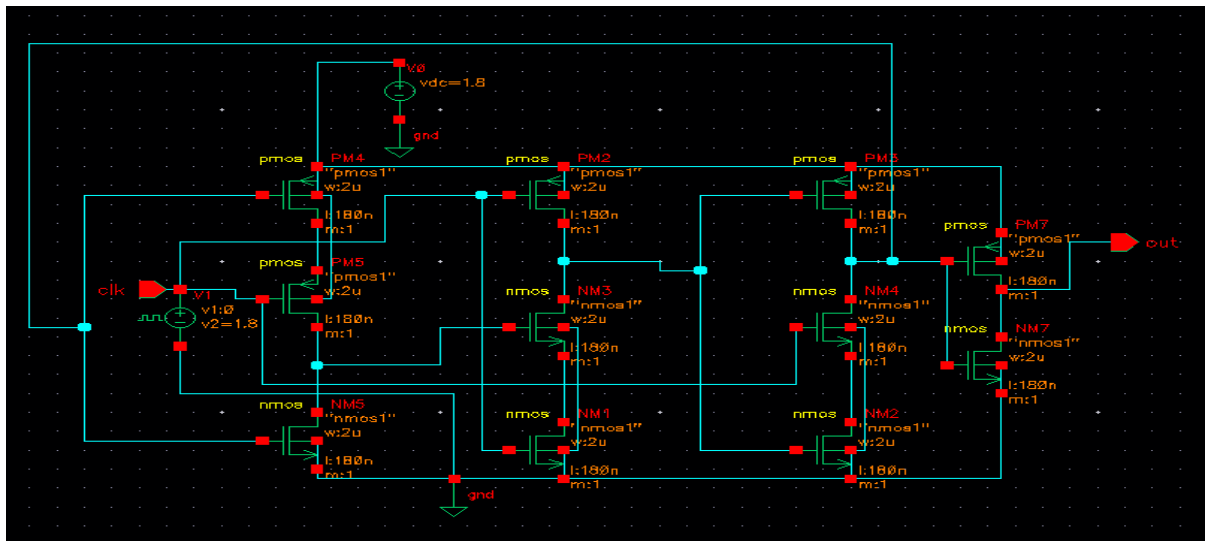

Figure 7: Circuit of TSPC based Divide-by-2 counter

4.5. Integration of phase-locked loop

After the implementation of every sub-block of the PLL such as the PFD, CP, LF, VCO and the divide-by-two counter, it is necessary to integrate the components to form a PLL system. The circuits mentioned prior are converted into a block using the cell-view option in the Cadence Virtuoso. This is done in order to provide a hassle-free connection of all the components. The proposed PLL is compared with the reference PLL (Sen and Jain 2014). Figure 8 provides a complete insight into PLL integrated using all the sub-components. PLL works in three modes namely the lock mode, capture mode and the free running mode. The PFD determines the phase difference between the input and the reference signals and then gives it to the charge pump as an input. The phase error is converted into a voltage and is given a boost by the charge pump. It is then applied to the loop filter where the noisy components are filtered out before the input is given to the VCO. The VCO produces a sinusoidal signal of a certain frequency and this is now given to the frequency divider and then, depending on the divider that is used in the circuit, the frequency is divided by that number N. The frequency of the VCO changes until its frequency is equivalent to the input frequency and it enters the lock mode.
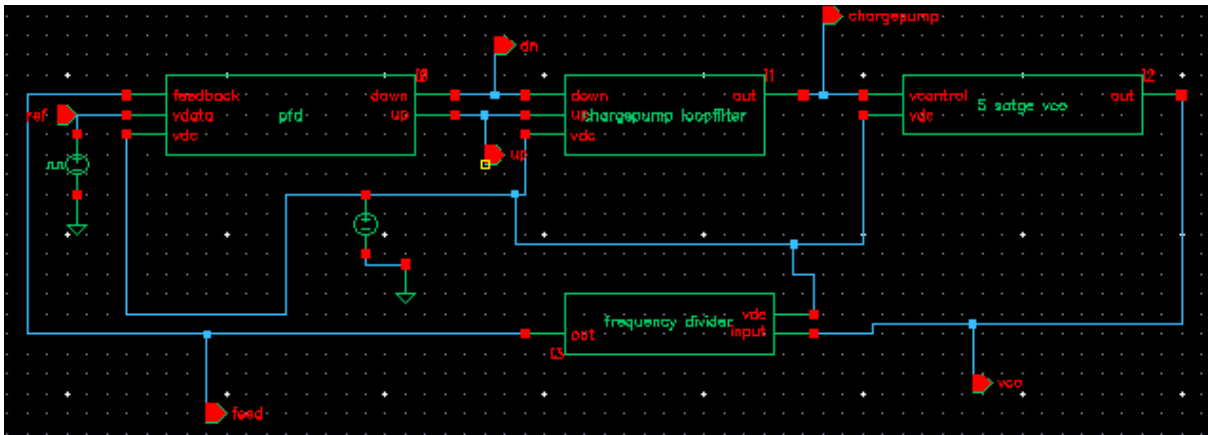
Figure 8: Circuit of the integrated PLL with all its sub components

5. Results and Discussions

The design of PLL and its subcomponents are discussed in the previous sections. Their simulation waveforms have also been observed using the Cadence Spectre. The simulation results and waveforms that are observed are discussed in this section.

5.1. Simulation results of the phase frequency detector

The simulation of the PFD circuits is performed in the frequency range of 100 kHz to 4 GHz with a supply voltage, set at 1.8 V. Simulation waveforms for the PFD without reset path is shown in Figure 9. The CLK_REF and CLK_VCO represent the first two waveforms where the clock signals are similar to another with the delay given to the latter waveform. Up and Down outputs are represented by the third and the fourth waveforms respectively. The performance analysis is done in terms of the transistor count and the power consumption.
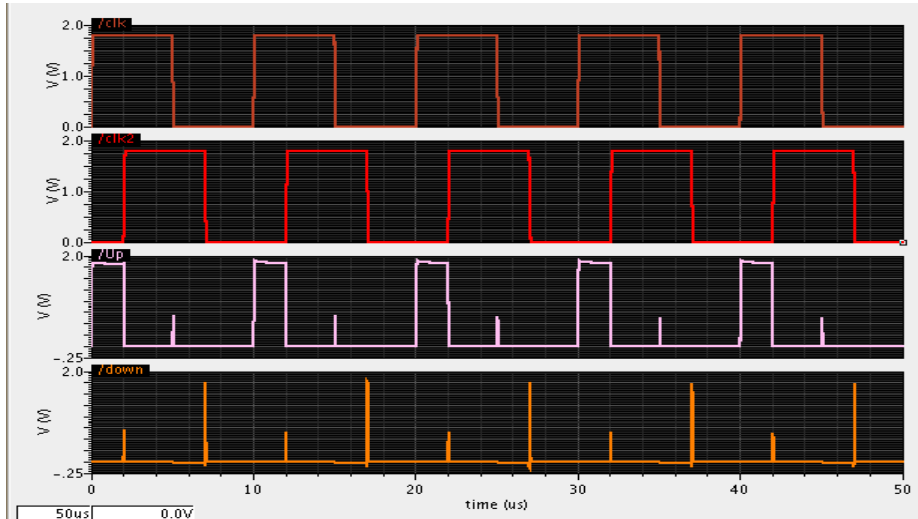

Figure 9: Simulation Waveform for PFD without reset path

The architecture of PFD from Thakore, Shah, and Devashrey (2019) and the proposed PFD without reset path are analyzed in the frequencies ranging from 1 to 4 GHz and results obtained are as presented in Figure 10. From Figure 10 it is inferred that the proposed PFD without reset consumes a power of 174 μW in comparison to that of Thakore, Shah, and Devashrey (2019) which consumes 356.5 μW at 1 GHz. A 50% reduction of power is observed. At lower frequencies, the proposed PFD without a reset path has a very slight effect on the reduction of power consumption, but as the frequency of operation changes to higher values, there is significant difference in the power consumption between the reference architecture in Thakore, Shah, and Devashrey (2019) and the proposed PFD without a reset path. The

changes that are made to the proposed design when compared to of the design in Thakore, Shah, and Devashrey (2019) is that the inverters used have the transistors sized at 5.2 μm (PMOS) and 3 μm (NMOS) whereas the proposed design has the transistors in the inverter sized at 2 μm a piece for both PMOS and NMOS.
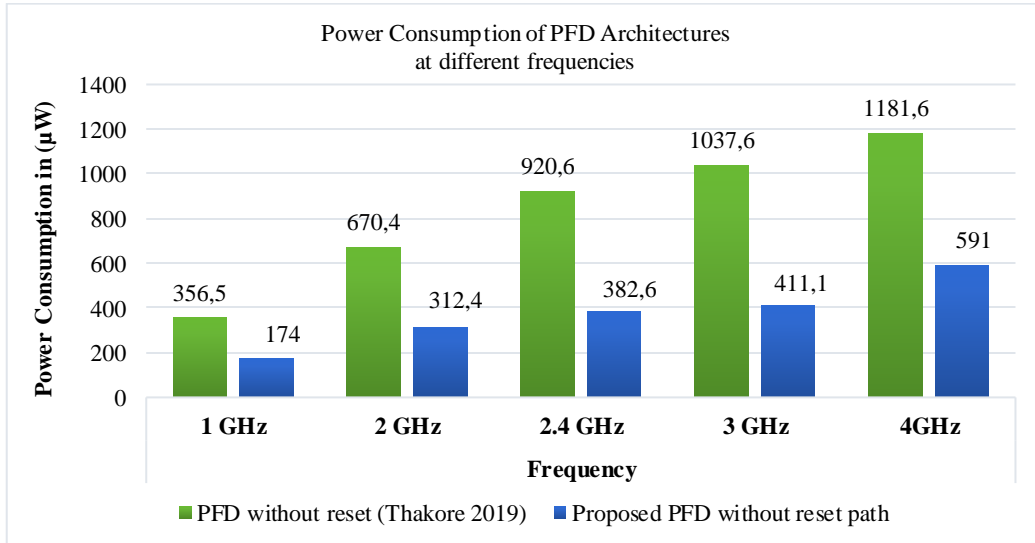

Figure 10: Comparison of power consumption of PFD architectures at different frequencies

5.2. Simulation results of the charge pump and loop filter

The simulation waveforms of the integrated charge pump and the loop filter are shown in Figure 11. The Up and Down signals are the outputs of the PFD and the resulting output signal is the expected output of the charge pump-loop filter integration.
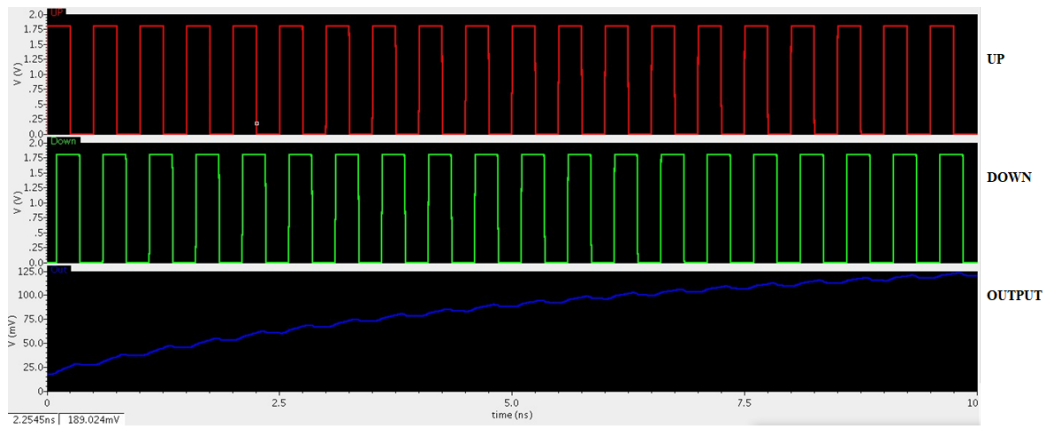

Figure 11: Simulation waveform of a charge pump integrated with a loop filter

Table 1 lists the simulation results of the charge pump-loop filter integration at 2 GHz and the power calculation. The proposed charge pump design with a transistor count of 16 with PMOS and NMOS each 8 in number, consumes 664.9 μW of power at 2 GHz frequency.

Charge Pump Circuits	Power Consumption (μW)	
	Without Loop Filter	With Loop Filter
Charge Pump with sizing (Praseetha, Benedict Tephila, and Anusuya 2019)	806.6	838.6
Charge Pump (Praseetha, Benedict Tephila, and Anusuya 2019)	705.5	710.6
Proposed Charge Pump	**659.5**	

Table 1: Power consumption of charge pump with loop filter at 2GHz

5.3. Simulation results of the VCO

The VCO circuit is simulated with a control voltage that is varied from 0.7 to 1.8 V to observe the operating frequencies in the different architectures. The transistor count is reduced and sizing is performed. The input controlling all the architectures is the control voltage which is as mentioned above and the output of the VCO is taken at the port "out". The initial oscillations in the VCO are started by giving a piecewise linear voltage to the output port and then the sinusoidal oscillations are obtained. The control voltage starts from 0.7 V, and increases up to 1.8 V. The increase in control voltage increases the frequency of operation. In the CSVCO (Sandhiya, Revathi, and Vinothkumar 2018) the frequency ranges from 1.247 to 2.425 GHz. The proposed VCO has an oscillation frequency ranging from 1.9 to 3.06 GHz. The proposed architecture has a greater frequency range when compared to that of conventional CSVCO. There is an increase in frequency of operation by 650 MHz. Table 2 represents the values of the control voltage versus frequency, which infers that in Sandhiya, Revathi, and Vinothkumar (2018) the output frequency is lesser when compared to the proposed VCO. At 1.8 V, the frequency of operation in Sandhiya, Revathi, and Vinothkumar (2018) is 2.425 GHz and the proposed VCO is 3.06 GHz. Figure 12 shows a comparison between the power consumption for the CSVCO, the pseudo NMOS based VCO and the proposed pseudo NMOS based VCO with sizing. The power consumption is reduced by 25.9 μW and 17 μW respectively in the proposed VCO compared to other VCO architectures. This trend can be seen up to a control voltage of 1.8 V.

VCO Architectures	CSVCO (Sandhiya, Revathi, and Vinothkumar 2018)	Pseudo NMOS (Belorkar and Ladhake 2010)	Proposed Pseudo NMOS VCO
Control Voltage (V)	Frequency (GHz)	Frequency (GHz)	Frequency (GHz)
0.7	1.2479	1.247	1.9
0.8	1.7915	1.69	2.42
0.9	2.0864	2.03	2.720
1.0	2.216	2.2	2.86
1.1	2.26	2.26	2.94
1.2	2.333	2.333	2.98
1.3	2.36	2.38	3.01
1.4	2.3816	2.42	3.02
1.5	2.397	2.44	3.04
1.6	2.4083	2.46	3.05
1.7	2.417	2.47	3.057
1.8	2.425	2.492	3.06

Table 2: Control Voltage versus Frequency for different architectures of VCO
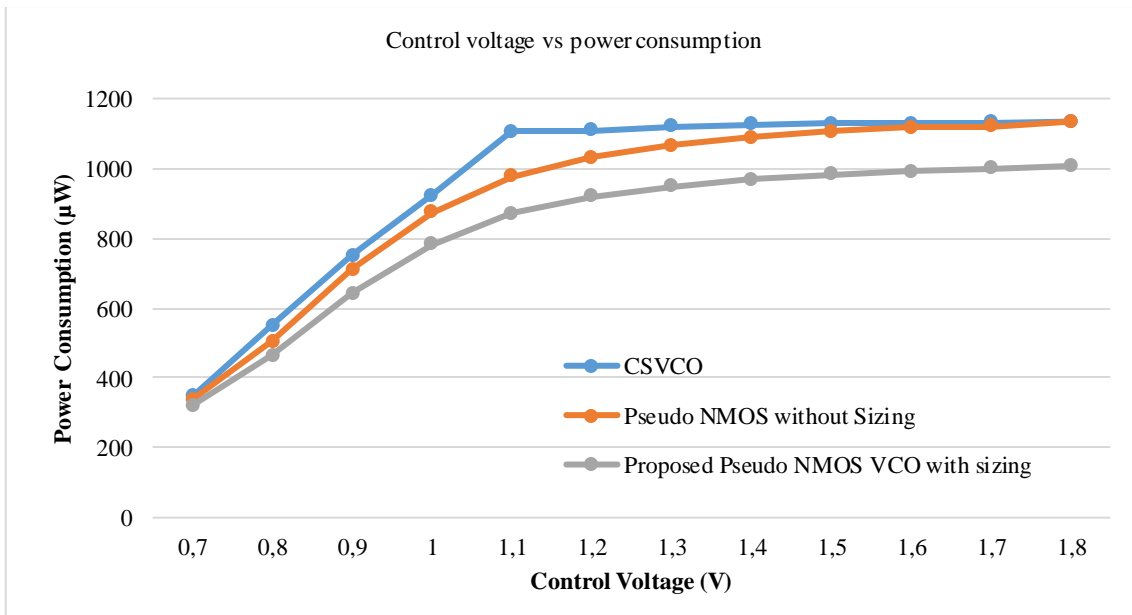
Figure 12: Comparison of power consumption for different VCO architectures

The term phase noise in a VCO is used to describe the random frequency fluctuations in the signal (Kumar 2016). The stability measures the extent to which an oscillator tends to maintain a constant frequency over a period of time. The phase noise characteristics of CSVCO and proposed pseudo NMOS are shown in Figure 13. The phase noise of CSVCO is -85.97 dBc/Hz at 1 MHz. There is an improvement in phase noise characteristics when pseudo NMOS based VCO is used in the circuit instead of CSVCO.
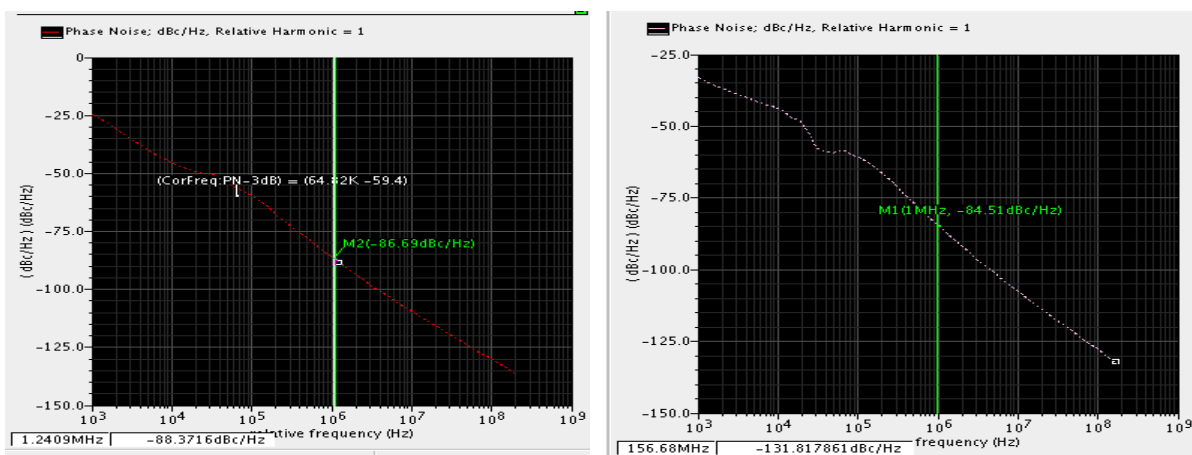
(a) Phase noise performance of CSVCO   (b) Phase noise performance of pseudo NMOS VCO

Figure 13 (a) and (b): The noise performance of the VCO architectures

5.4. Simulation results of the frequency divider

A divide-by-2 counter is used as a frequency divider. The TSPC based D flip-flop used in the circuit is more compact and the clock skew problem is also eliminated. The output of the VCO is provided to the frequency divider. The frequency of the input signal is divided by a factor of 2. The power consumption of the frequency divider at different frequencies is tabulated and shown in Table 3. The input frequency is varied from 1 MHz to 4 GHz and the supply voltage is fixed at 1.8 V. Power calculation of every frequency is tabulated. For the center frequency of 2 GHz the output frequency of the frequency divider is 1.0013 GHz and it consumes a power of 188.8 μW.
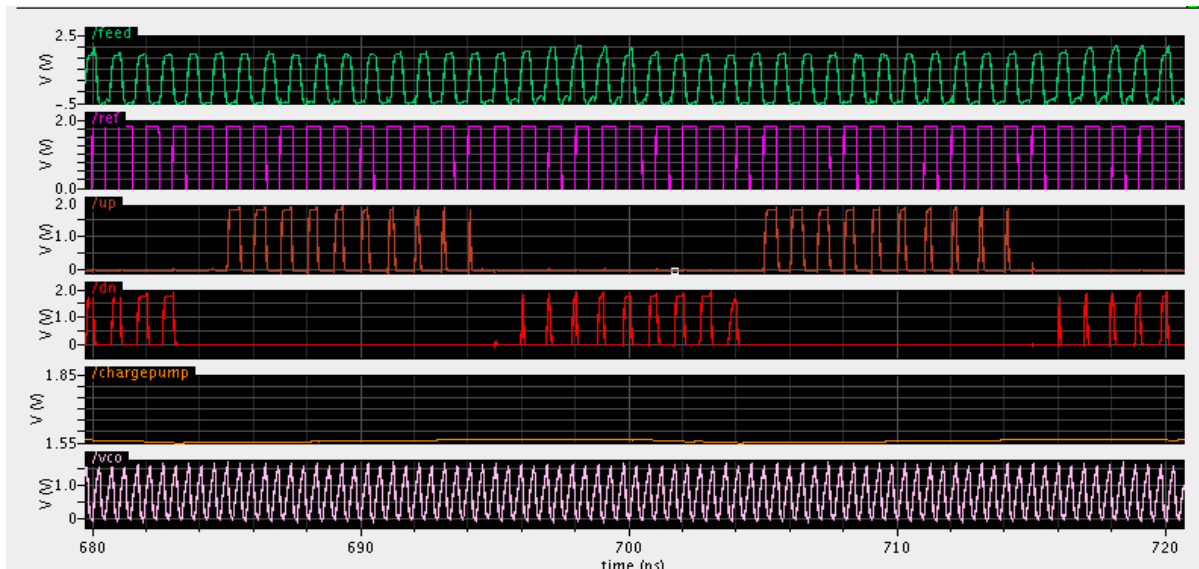
VCO Output Frequency	Counter output Frequency	Power (µW)
1 MHz	500.9 kHz	0.24
10 MHz	5.02 MHz	2.3
100 MHz	49.99 MHz	9.022
1 GHz	500.4 MHz	94.27
2 GHz	1.0013 GHz	188.8
4 GHz	1.99 GHz	362.1

Table 3: Power consumption of Divide by 2 Counter at different frequencies

5.5. Simulation results of the integrated PLL

The PLL is the circuit integrated using the designed PFD, charge pump, loop filter, VCO, and the frequency divider. Figure 14 shows the simulation waveform at every stage of the integrated PLL namely reference frequency which is the input, the PFD outputs namely the Up and Down, the output of the CP, LF, VCO, frequency divider, which is given as feedback and as one of the inputs to the PFD. The circuits for both the reference PLL (Sen and Jain 2014) and the proposed PLL simulated from an input frequency of 50 MHz to a value of 4 GHz. In order to provide an initial setup for the circuit, the initial configuration was set at a voltage of 1.8 V for the feedback signal. This enables the PLL to find an initial condition based on which the functioning begins.

The input frequency varied from 500 MHz to 4 GHz and the corresponding power values along with the output frequencies are noted. At a frequency of 500 MHz, the output of the VCO had a frequency of 1.96 GHz, the feedback frequency being half of the VCO output that is 0.98 GHz in case of the reference PLL. In the proposed PLL, the frequency of VCO output was 2.09 GHz and thereby the feedback frequency being 1.045 GHz. This indicates an increase of 130 MHz in terms of frequency in the proposed PLL when compared to the reference PLL.

Figure 14: Simulation waveform of the proposed PLL

The Figure 15 represents the comparison between the frequencies plotted against the VCO output frequencies. It can be inferred from Figure 15 that for the reference frequency ranging from 50 MHz to 4 GHz, output frequencies range from 1.96 to 2.04 GHz for the reference PLL architecture (Sen and Jain 2014) and range from 2.09 to 2.116 GHz for the proposed PLL architecture. This increase in frequency is an added advantage. The power consumption values in the reference PLL architecture (Sen and Jain 2014) and the proposed architecture are indicated in Figure 16. The power consumption at a reference frequency of 2 GHz had

produced an increase of 125 MHz in terms of the output frequency and a decrease of 129 µW of power which is significant for a low-power application. This being the main motive of the work, it can be inferred that the proposed PLL is power efficient.

The range of frequencies over which the PLL will track the input frequency signal and remain locked is referred to as PLL lock range. The lock range is usually a band of frequencies above and below the PLL free running frequency. If the frequency of the input signal is outside the PLL lock range then PLL will not lock. The range of input frequencies over which PLL will capture the input signal is referred to as PLL capture range. Lock range is always greater than the capture range. The total time taken by the PLL to establish a lock is called the pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.
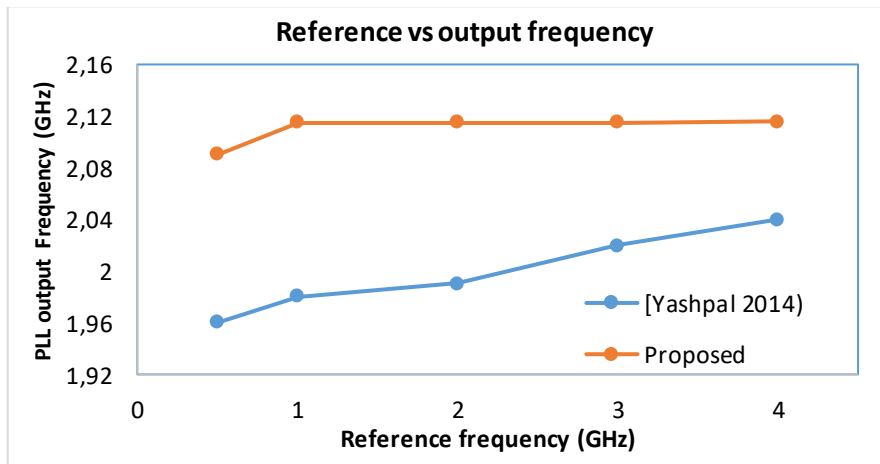

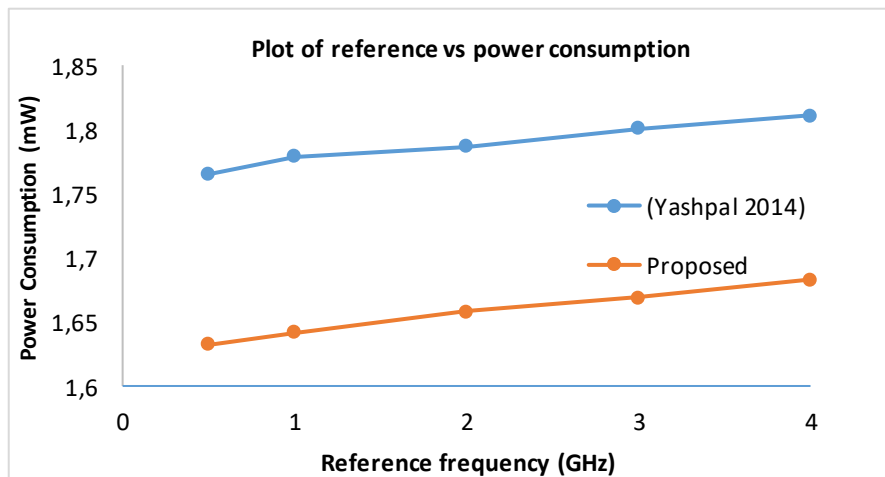**Figure 15**: Reference frequency vs PLL output frequency

Figure 16: Reference frequency vs power consumption of PLL architectures

The parameters measured for the proposed PLL are as follows. The range of the input frequency was up to 4 GHz, tuning range of the VCO was from 1.9 to 3.06 GHz and gain of the VCO was 1.0545 GHz/V. The free- running frequency of the PLL is 2.115 GHz, the capture range is from 2.09 to 2.14 GHz. The lock range of the PLL ranges from 1 to 3.5 GHz and the lock time of the PLL is 508 ns.

6. Conclusion

A design and implementation of the power efficient PLL architecture is proposed in order to increase the power efficiency and reduce area. To design a PLL of this nature, the sub-

components' architectures must be power efficient. The proposed PFD without reset path has an improvement of 50 % in terms of power at a frequency range of 1 to 4 GHz. The proposed charge pump with loop filter is 10% more power efficient as compared to the existing architecture. The proposed pseudo NMOS based VCO has an improvement of 25.9 µW in terms of power and also 650 MHz in terms of frequency of operation. The divide-by-counter is also power efficient. The PLL integrated using the different sub-components when compared with the existing architecture functions at an input frequency of 2 GHz and has a reduction of 129 µW in terms of power and an increase in the output frequency by 116 MHz. The capture range and lock range of the proposed PLL ranges from 2.09 to 2.14 GHz and 1 to 3.5GHz respectively. For a PLL it is necessary to operate at high frequency with low power consumption, the proposed PLL achieves both. There is no trade-off between the frequency of operation and power. The proposed PLL has an advantage in terms of both high frequency operation as well as power efficiency. The proposed low-power PLL design can be employed in applications that employ a high frequency of operation, thus reducing the power consumption at an increased frequency of operation.

References

Anirvinnan, P., V. S. Parashar, D. A. Bharadwaj, and B. S. Premananda. 2019. "Low power AVLS-TSPC based 2/3 pre-scaler". *International Journal of Engineering and Advanced Technology* 9, no. 1 (october): 6687-93. https://doi.org/10.35940/ijeat.A1974.109119.

Belorkar, U. A., and S. A. Ladhake. 2010. "High performance voltage controlled oscillator (VCO) using 65NM VLSI technology". *International Journal of Computer Networks & Communications* 2, no. 4 (july): 73-82. https://doi.org/10.5121/ijcnc.2010.2407.

Bency, M., S. R. Prasanna, G. P. Shreya, and B. S. Premananda. 2021. "PFD with dead zone based low power modified phase lock loop using AVLS technique". In *Proceedings - 2021 6th International Conference on Communication and Electronics Systems (ICCES)*, 212-17. IEEE. https://doi.org/10.1109/ICCES51350.2021.9489216.

Das, M., P. Mostafa, A. Pal, D. Das, and S. Chatterjee. 2018. "Design of an energy efficient, low phase noise current-starved VCO using pseudo-NMOS logic". In *Advances in Communication, Devices and Networking*, 35-42. Lecture Notes in Electrical Engineering, vol. 462. Springer Singapore. https://doi.org/10.1007/978-981-10-7901-6_5.

Ghaderi, N., H. R. Erfani-jazi, and M. Mohseni-Mirabadi. 2016. "A low noise, low power phase-locked loop, using optimization methods". *Journal of Electrical and Computer Engineering* 2016: Article ID 8202581. https://doi.org/10.1155/2016/8202581.

Kaipu, S. V. R., K. Vaish, S. Komatireddy, A. Sood, and M. Goswami. 2016. "Design of a low power wide range phase locked loop using 180nm CMOS technology". In *2016 International Conference on Signal Processing and Communication (ICSC)*, 443-47. IEEE. https://doi.org/10.1109/ICSPCom.2016.7980621.

Kumar, M. 2016. "VCO design using NAND gate for low power application". *Journal of Semiconductor Technology and Science* 16, no. 5 (october): 650-56. https://doi.org/10.5573/JSTS.2016.16.5.650.

Nanda, U., D. P. Acharya, and S. K. Patra. 2013. "Design of a low noise PLL for GSM application". In *Proceedings - 2013 International Conference on Circuits, Controls and Communications, CCUBE 2013*, Article number 6718578. IEEE. https://doi.org/10.1109/CCUBE.2013.6718578.

Nargund, A. A., C. M. A. Kashyap, D. Prashanth, B. S. Premananda, and A. Sharma. 2016. "A novel method of wideband acquisition and anti-sideband lock in PM receivers using FFT".

In *Proceedings - 2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, 2098-101. IEEE. https://doi.org/10.1109/RTEICT.2016.7808209.

Praseetha, S., M. Benedict Tephila, and S. Anusuya. 2019. "Implementation of phase frequency detector in phase locked loop using preset able modified TSPC D flip-flop". *International Journal of Innovative Technology and Exploring Engineering* 8, no. 12 (october): 977-80. https://doi.org/10.35940/ijitee.J9828.1081219.

Ravisaheb, H. B., and B. H. Nagpara. 2017. "Design and implementation of phase frequency detector using different logic gates in 45nm CMOS process technology". *International Research Journal of Engineering and Technology* 4, no. 2 (february): 189-93.

Sandhiya, S., S. Revathi, and B. Vinothkumar. 2018. "Design of voltage controlled oscillator in 180nm CMOS technology". *International Research Journal of Engineering and Technology* 5, no. 3: 844-49.

Sen, Y., and N. Jain. 2014. "Design and implementation of phase locked loop using current starved voltage controlled oscillator". *Advance in Electronic and Electric Engineering* 4, no. 6: 637-44.

Thakore, K. P., K. Shah, and N. M. Devashrey. 2019. "Design and implementation of low power phase frequency detector for phase lock loop". In *Proceedings - 2019 3rd International Conference on Computing Methodologies and Communication (ICCMC)*, 644-47. https://doi.org/10.1109/ICCMC.2019.8819745.