U.Porto Journal of Engineering, 7:4 (2021) 33-45
ISSN 2183-6493
DOI: 10.24840/2183-6493_007.004_0003

Received: 18 July, 2021
Accepted: 21 September, 2021
Published: 26 November, 2021

Design of Low Voltage Quasi-floating Self Cascode Current Mirror

P. Anil Kumar[1], S. Tamil[2], N. Raj[3]

[1]Department of ECE, Sarvepalli Radhakrishnan University Bhopal, India (anilpole403@gmail.com) ORCID 0000-0002-0076-0355; [2]Department of ECE, Sarvepalli Radhakrishnan University Bhopal, India (stamil2005@gmail.com); [3]Department of ECE, The LNM Institute of Information Technology Jaipur, India (nikhilpub@gmail.com) ORCID 0000-0002-7544-9385

Abstract

In this paper, a modified structure of self-cascode structure is proposed. In the proposed structure, the MOSFET working in saturation mode is replaced by a Quasi-floating gate MOSFET by which the threshold voltage can be scaled, resulting in an increase in the drain-to-source voltage of other MOSFET operating in the linear region. The increased drain-to-source voltage results in a change in the operating region, which here is from linear to saturation regime. To exploit the performance of the proposed structure, the design of the current mirror circuit is shown in this paper. The proposed architecture when compared with its conventional design showed improvement in performance without affecting the other parameters. The complete design is done using MOSFET models of 180nm technology using Spice at supply dual supply of 0.5V.

Author Keywords. Self Cascode, Quasi-floating Gate, Current Mirror, Transconductance, Output Impedance, Bandwidth.

Type: Research Article
Open Access Peer Reviewed CC BY

1. Introduction

The nanometer device dimensions and sub-volt operations have favored the design of high performance digital logic functions. But these devices do not provide satisfactory performance in the case of designing analog circuits which is mainly due to channel length modulation (CLM) effect. Among various approaches, the self cascode (SC) MOSFET is widely adopted to reduce the CLM effect (Galup-Montoro, Schneider, and Loss 1994; Gerosa and Neviani 2003). However, the SC structure has a disadvantage of having requirement of large device dimensions. Many solutions have been introduced to compensate such requirements such as Asymmetric threshold voltage (V_{th}) based SC structure (Fujimori and Sugimoto 1998) dual-work function-gate (DWFG) MOSFET & Zero threshold (ZVT) MOSFET (Na, Baek, and Kim 2012), forward body-biasing technique (Baek, Na, and Kim 2016), etc. However, in such an approach there is a requirement of additional or complicated fabrication processing steps (Baek et al. 2013).

The threshold voltage has been continuously an obstacle in circuit design, especially for low voltage analog circuits. The reason behind this is due to the fact that the scaling technique is not applicable on the threshold voltage. In this regard, the minimum supply voltage cannot be scaled below the threshold voltage of MOSFET. Few widely adopted low voltage (LV) low power (LP) techniques that have proved its potential are level shifter technique (Rajput and Jamuar 2001), Bulk Driven technique (Blalock, Allen, and Rincon-Mora 1998), Floating Gate (FG) structure (Hasler and Lande 2001), Quasi-floating Gate (QFG) structure (Ramirez-Angulo

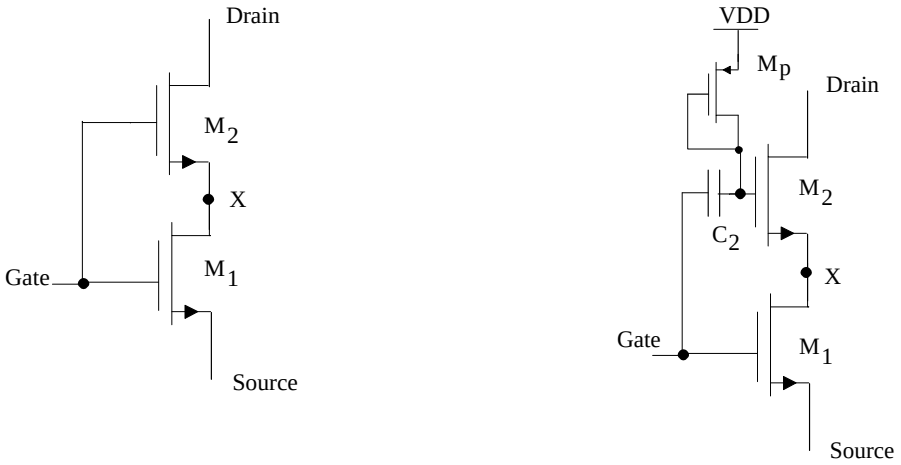
et al. 2003; Ramirez-Angulo et al. 2004), and Bulk driven floating/quasi-floating Gate (BDFG/BDQFG) structure (Khateb 2014, 2015). These LV LP techniques are categorized as non-conventional techniques. However, the associated drawback of using these techniques is in terms of low transconductance & thus low bandwidth circuits compared to gate driven (GD) MOSFET based designs. Among the aforementioned techniques, FG and its modified design QFG has proven its potential in LV analog design by providing multi-input capacitive connection which favored scaling of the threshold voltage. Apart from this, when QFG combined with BD technique resulting in structure popularly known as BDQFG MOSFET showed improved frequency parameters over of simple BD based designs. Generally, BD based designs offer very low voltage operation but do suffer from poor linearity & extremely low transconductance. So, depending upon the desired performance parameter enhancement of designs, the technique choices are made. For example- few widely cited current mirror circuits reported in the literature based on aforementioned non-conventional techniques can be found as: based on BD (Zhang and El-Masry 2004; Aggarwal, Gupta, and Gupta 2013; Raj et al. 2016a), based on FG (Sharma et al. 2006; Manhas et al. 2008), based on QFG (Lopez-Martin et al. 2008; Esparza-Alfaro et al. 2012; Esparza-Alfaro et al. 2014; Raj et al. 2014a), and based on BDQFG (Raj et al. 2014b, 2016b, 2016c, 2017; Bchir, Aloui, and Hassen 2020).

In this paper, a modified structure of gate driven Self Cascode (SC) is proposed which uses the Quasi floating gate (QFG) MOSFET. The proposed QFG-SC structure results in the operation of both the MOSFETs in saturation mode. This results in improved performance over conventional gate driven SC structure. Further to evaluate the performance of the proposed QFG-SC, the current mirror design is presented and compared with its conventional architecture.

The paper is divided in five sections. Section 2 details on the proposed QFG-SC structure followed for the design of the basic current mirror circuit based on the proposed QFG-SC and as well based on conventional SC structure in section 3. The current mirror designs are supported by their small-signal analysis. The simulation results are discussed in section 4 followed by the conclusion in section 5.

2. Proposed QFG Self Cascode

A modified structure of SC based on QFG MOSFET is proposed in this section. Figure 1(a) and Figure1(b) are the conventional and proposed QFG-SC structures.



(a) (b)

Figure 1: Self cascode structure: (a) Conventional SC; (b) Modified QFG-SC

Here in Figure 1(a), M_1 operates in linear mode whereas M_2 in saturation mode. As known the transconductance achieved is maxima when MOSFET operates in saturation so by changing M_1 to saturation mode the effective transconductance of the SC structure can be enhanced which can be used in the design of high gain circuits. If $V_{th,M2}<V_{th,M1}$ is achieved then a possibility to increase V_{DS} of M_1 can be achieved. The necessary condition required to be satisfied for operating both the MOSFETs of SC in the saturation region is:

$$V_{DS,sat.M_2} \geq V_{th,M_1} - V_{th,M_2} \quad (1)$$

To satisfy the condition of (1), QFG is used in the proposed SC design as shown in Figure 1(b) where MOSFET M_2 is converted into QFG MOSFET. The effective threshold voltage of M_2 changes to

$$V_{th2,eff} = \frac{C_{T,qfg}}{C_2} V_{th2} - \frac{C'_{GD,MP}}{C_2} V_{DD} \quad (2)$$

where $C_{T,qfg}$ is the total capacitance seen at the QFG node of M_2 and $C'_{GD,MP}$ is the parasitic capacitance of M_P. The capacitor C_2 and MOSFET M_P is used to realize M_2 in QFG mode. As seen in (2), the effective threshold of M_2 gets scaled down which increases the possibility of satisfying the condition of (1) and the MOSFET M_1 enters into saturation. As both the MOSFETs of SC turns in saturation, the effective transconductance gets increased. The analysis of the proposed QFG-SC structure of Figure 1(b) is shown below with its small-signal model shown in Figure 2.

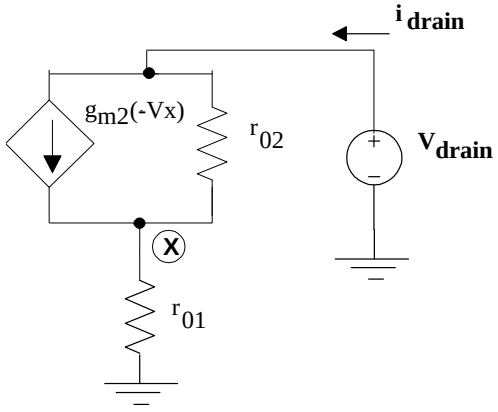


Figure 2: Small-signal model of proposed QFG-SC structure

At drain terminal

$$i_{drain} = g_{m2}(-V_X) + \frac{V_{drain} - V_X}{r_{02}} \quad (3)$$

Also

$$V_X = r_{01} i_{drain} \quad (4)$$

From (3) and (4)

$$i_{drain} = g_{m2}(-r_{01} i_{drain}) + \frac{V_{drain} - r_{01} i_{drain}}{r_{02}} \quad (5)$$

Solving (5)

$$r_0 = \frac{V_{drain}}{i_{drain}} = r_{02} + g_{m2} r_{02} r_{01} + r_{01} \quad (6)$$

Since $g_m r_0 >> 1$

From (6)

$$r_0 = r_{02}\left(1+g_{m2}r_{01}\right)+r_{01} \approx g_{m2}r_{01}r_{02}+r_{01} \tag{7}$$

$$r_{0,QFG-SC} \approx g_{m2,qfg}r_{02,qfg}r_{01} \tag{8}$$

Similarly performing the analysis of conventional SC structure shown in Figure 1(a),

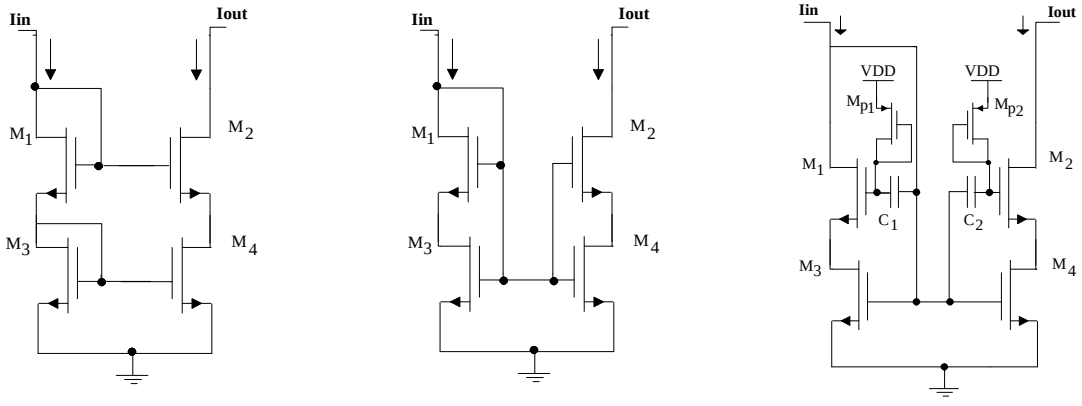
$$r_{0,SC} = \left(1+\frac{g_{m2}}{g_{m1}}\right)r_{02} \tag{9}$$

Comparing (8) and (9), the advantage of using the QFG technique in self-cascode can be easily observed in terms of the significant increase in resistance, approximately equal to that of a cascode. The effective transconductance of the proposed QFG-SC is calculated as:

$$G_{m,QFG-SC} = \frac{g_{m1}r_{01}+g_{m2,qfg}r_{02,qfg}+g_{m1}g_{m2,qfg}r_{01}r_{02,qfg}}{r_{01}+r_{02,qfg}+g_{m2,qfg}r_{01}r_{02,qfg}} \tag{10}$$

3. Proposed Current Mirror

Current mirror (CM) is a circuit that generates the output as a replica of input current at a high impedance node so as to avoid the constant current irrespective of the type of load. Current mirror with wide operating range, better bandwidth, low input, and high output resistances are some of the key requirements. The gate driven cascode current mirror which fulfills the current mirror requirements is shown in Figure 3(a). The input MOSFETs M_1 and M_3 are configured as diode connected. The input current and output current is shown by i_{in} and i_{out} respectively. The output resistance is boosted by the intrinsic gain of cascode MOSFET M_1, i.e. by $g_m r_0$. However, such CM suffers from poor voltage swing. Yet another configuration, self cascode provides the same feature with better swing. The schematic of the current mirror design based on conventional SC and based on proposed QFG-SC is shown in Figure 3(b) and Figure 3(c) respectively. In Figure 3(b), the MOSFET pairs (M_1, M_3) and (M_2, M_4) are the conventional SC structures. Here MOSFETs M_1 and M_2 operate in the saturation region whereas the MOSFETs M_3 and M_4 operate in the linear mode. In the proposed current mirror shown in Figure3(c), the MOSFETs M_1 and M_2 are replaced which in this case are QFG MOSFETs. The capacitors C_1 and C_2 along with cut-off region MOSFETs M_{P1} and M_{P2} respectively change the gate terminals of MOSFETs M_1 and M_2, respectively, in QFG.



(a) (b) (c)

Figure 3: Current Mirror: (a) Cascode CM; (b) Conventional SC CM; (c) Proposed QFG SC CM

From the analysis of the standard current mirror, it has been observed that the input resistance is inversely proportional whereas the output resistance is directly proportional to

the transconductance of MOSFETs used for current mirroring purpose. So, in Figure 3(b), by changing the mode of operation of M_3 from linear to saturation enhances the transconductance of the SC which helps in reducing the input resistance and also the similar effect on M_4 enhances the output resistance. These conditions were achieved by using QFG MOSFET M_1 and M_2 as shown in Figure 3(c).

3.1. Small signal analysis

The small signal analysis in terms of input resistance, output resistance, and bandwidth of current mirror based on proposed QFG-SC is carried out and also compared with that of based on conventional SC structure and standard cascode structure. The symbols used throughout the analysis are the standard spice model parameters of MOSFET and have their usual meaning.

3.1.1. Input resistance

The small signal model for calculating the input resistance ($R_{in,QFG-SC}$) of the proposed current mirror is shown in Figure 4.

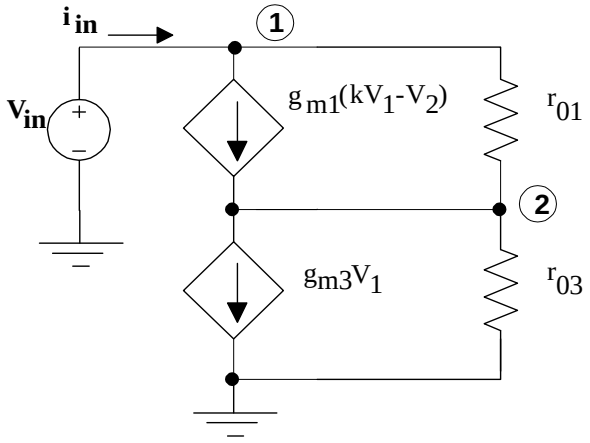


Figure 4: Small signal model for calculating input resistance

At node 1,

$$i_{in} = g_{m1}\left(kV_1 - V_2\right) + \frac{V_1 - V_2}{r_{01}} \tag{11}$$

At node 2,

$$i_{in} = g_{m3}V_1 + \frac{V_2}{r_{03}} \tag{12}$$

Solving for V_2

$$V_2 = \left(i_{in} - g_{m3}V_1\right)r_{03} \tag{13}$$

From (11) and (13)

$$i_{in} = \left(kg_{m1} + \frac{1}{r_{01}}\right)V_1 - \left(g_{m1} + \frac{1}{r_{01}}\right)\left(i_{in} - g_{m3}V_1\right)r_{03} \tag{14}$$

Solving (14)

$$R_{in,QFG-SC} = \frac{V_1}{i_{in}} = \frac{r_{01} + r_{03} + g_{m1}r_{01}r_{03}}{1 + kg_{m1}r_{01} + g_{m3}r_{03} + g_{m1}g_{m3}r_{01}r_{03}} \tag{15}$$

Since $g_m r_0 >> 1$

From (15)

$$R_{in,QFG-SC} = \frac{r_{01} + (1 + g_{m1} r_{01}) r_{03}}{1 + k g_{m1} r_{01} + (1 + g_{m1} r_{01}) g_{m3} r_{03}} \quad (16)$$

Simplifying

$$R_{in,QFG-SC} \approx \frac{g_{m1} r_{01} r_{03}}{g_{m1} r_{01} g_{m3} r_{03}} \approx \frac{1}{g_{m3}} \quad (17)$$

Similary, the input resistance of conventional SC based current mirror is given by

$$R_{in,conv.-SC} \approx \frac{g_{m3} + g_{m1}}{g_{m3} g_{m1}} = \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \quad (18)$$

whereas for cascode it is given by Aggarwal, Gupta, and Gupta (2013)

$$R_{in,cascode} \approx \frac{g_{m3} + g_{m1}}{g_{m3} g_{m1}} = \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \quad (19)$$

Comparing (17), (18), and (19), it is observed that the proposed current mirror's input resistance gets reduced by $1/g_{m1}$.

3.1.2. Output resistance

The small signal model for calculating the output resistance ($R_{out,QFG-SC}$) of the proposed current mirror is shown in Figure 5.

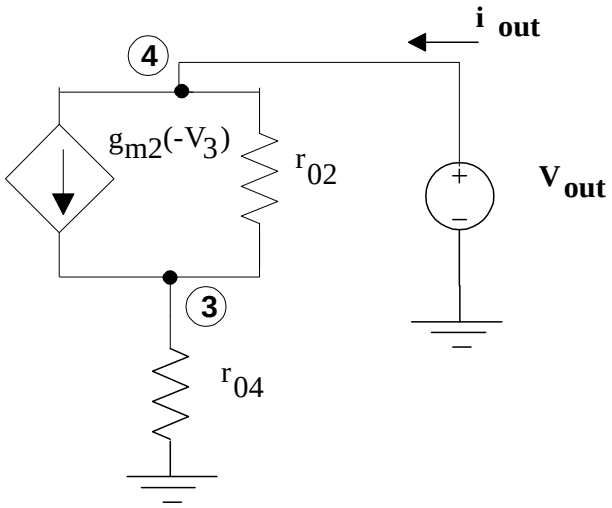


Figure 5: Small signal model for calculating output resistance

At node 4,

$$i_{out} = -\left(g_{m2} + \frac{1}{r_{02}} \right) V_3 + \frac{V_4}{r_{02}} \quad (20)$$

At node 3,

$$V_3 = r_{04} i_{out} \quad (21)$$

From (19) and (20)

$$i_{out} = -\left(g_{m2} + \frac{1}{r_{02}} \right) i_{out} r_{04} + \frac{V_4}{r_{02}} \quad (22)$$

Simplifying

$$R_{out,QFG-SC} = \frac{V_4}{i_{out}} = r_{02} + r_{04} + g_{m2} r_{02} r_{04} \quad (23)$$

Since $g_m r_0 >> 1$

From (23)

$$R_{out,QFG-SC} = r_{02} + (1 + g_{m2} r_{02}) r_{04} \approx r_{02} + g_{m2} r_{02} r_{04} \quad (24)$$

Simplifying

$$R_{out,QFG-SC} \approx g_{m2,qfg} r_{02,qfg} r_{04} \quad (25)$$

Similarly, the output resistance of conventional SC based current mirror is given by

$$R_{out,conv.-SC} = \frac{1 + (g_{m4} + g_{m2}) r_{02}}{g_{m4}} \approx \left(1 + \frac{g_{m2}}{g_{m4}}\right) r_{02} \quad (26)$$

whereas for cascode it is given by Aggarwal, Gupta, and Gupta (2013)

$$R_{out,cascode} = r_{04} + r_{02} + g_{m2} r_{02} r_{04} \approx g_{m2} r_{02} r_{04} \quad (27)$$

Comparing (25), (26), and (27), it can be observed that for the proposed QFG SC based current mirror the output resistance is almost equal to that of cascode but compared to the conventional SC structure, it is boosted approximately by ($g_{m2}r_{04}$) factor.

3.1.3. Bandwidth

The small signal model for calculating bandwidth is shown in Figure 6. The output conductance and the C_{gd} effects are neglected in comparison to C_{gs} of the saturation mode transistors.

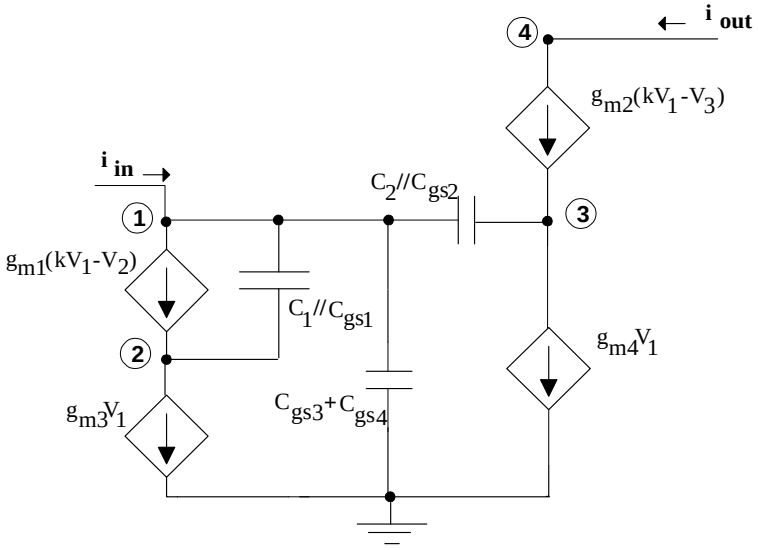


Figure 6: Small signal model for calculating bandwidth

At node 1,

$$i_{in} = g_{m1}(kV_1 - V_2) + s(C_1 // C_{gs1})V_{12} + s(C_{gs3} + C_{gs4})V_1 + s(C_2 // C_{gs2})V_{13} \quad (28)$$

At node 2,

$$g_{m1}(kV_1 - V_2) + s(C_1 // C_{gs1})V_{12} = g_{m3}V_1 \quad (29)$$

From (28) and (29)

$$i_{in} = g_{m3}V_1 + s(C_{gs3} + C_{gs4})V_1 + s(C_2 // C_{gs2})V_{13} \quad (30)$$

At node 4,

$$i_{out} = g_{m2}(kV_1 - V_3) \quad (31)$$

At node 3,

$$g_{m2}(kV_1 - V_3) = g_{m4}V_1 + s(C_2 // C_{gs2})V_{31} \quad (32)$$

From (30), (31), and (32), solving for current gain

$$\frac{i_{out}}{i_{in}} = \frac{g_{m4}g_{m2}}{g_{m3}g_{m2} + s\begin{pmatrix}(g_{m3}+g_{m4})(C_2 //C_{gs2})+\\ g_{m2}(C_{gs3}+C_{gs4})\end{pmatrix} + s^2(C_{gs3}+C_{gs4})(C_2 //C_{gs2})} \quad (33)$$

$$A_{I,QFG-SC} = \frac{g_{m4}g_{m2}/(C_{gs3}+C_{gs4})(C_2 //C_{gs2})}{s^2 + s\left(\frac{g_{m3}+g_{m4}}{C_{gs3}+C_{gs4}} + \frac{g_{m2}}{C_2 //C_{gs2}}\right) + \frac{g_{m3}g_{m2}}{(C_{gs3}+C_{gs4})(C_2 //C_{gs2})}} \quad (34)$$

Assume $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$ and $C_{gs1} = C_{gs2}$,

From (34)

$$\omega_{0,QFG-SC} = \sqrt{\frac{g_{m1}g_{m3}}{(C_1 //C_{gs1})(C_{gs3}+C_{gs4})}} \quad (35)$$

Similarly solving for current gain of conventional SC based current mirror

$$A_{I,conv.-SC} = \frac{g_{m1}g_{m3}/C_{gs1}(C_{gs3}+C_{gs4})}{s^2 + s\left(\frac{2g_{m3}}{C_{gs3}+C_{gs4}} + \frac{g_{m1}+g_{m3}}{C_{gs1}}\right) + \frac{g_{m1}g_{m3}}{C_{gs1}(C_{gs3}+C_{gs4})}} \quad (36)$$

From (36)

$$\omega_{0,conv.-SC} = \sqrt{\frac{g_{m1}g_{m3}}{C_{gs1}(C_{gs3}+C_{gs4})}} \quad (37)$$

From (25) and (37), a slight variation in the bandwidth can be observed. However, the same remains for that of cascode.

4. Simulation Results

The device dimensions taken for simulation purposes for current mirror designs of Figure 3 are shown in Table 1. The channel length of the transistors is kept at its minimum value. The other assumed parameters for circuit simulations are also listed. The simulation results well support the mathematical analysis of the proposed design.

Transistors	W (µm)	L (µm)	Transistors	W (µm)	L (µm)
M1	5	0.24	M4	5	0.24
M2	5	0.24	MP1	0.24	0.24
M3	5	0.24	Mp2	0.24	0.24
C1=C2=1pf, supply=± 0.5V					

Table 1: Device dimension MOSFETs

The current transfer characteristic curve and their current copying accuracy error percentage for the input current ranging from 0 to 500uA are shown in Figure 7 and Figure 8 respectively.

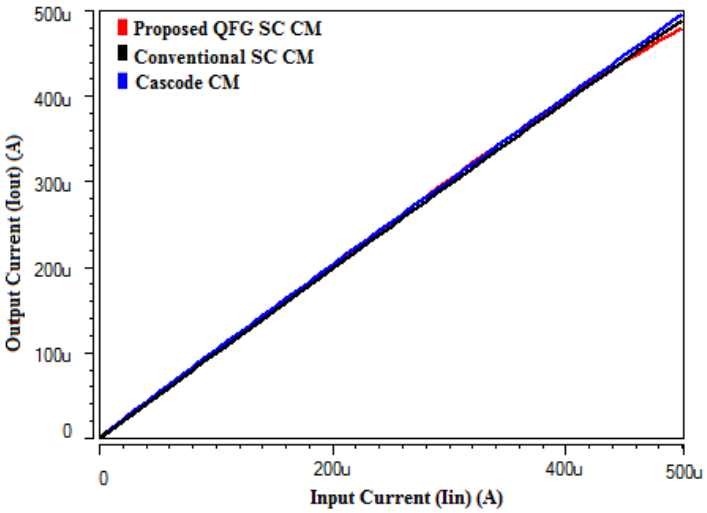


Figure 7: Transfer characteristics

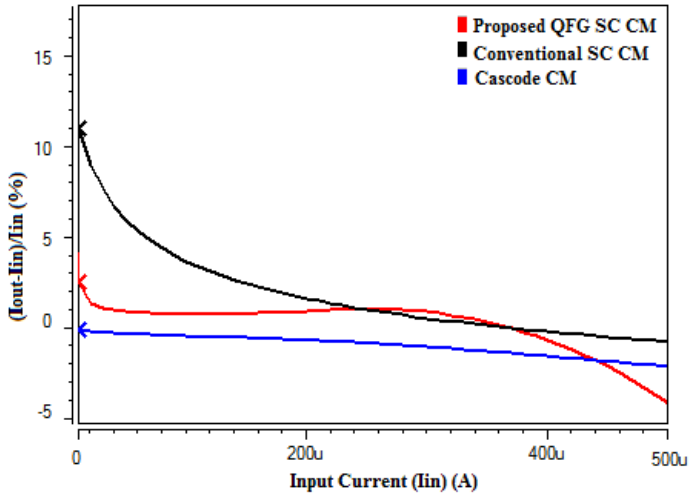


Figure 8: Error in current transfer characteristics

The minimum error is found for the proposed QFG-SC current mirror circuit when compared to its conventional design. The input characteristic over input current ranging from 0 to 500uA is shown in Figure 9 where the disadvantage of using cascode when it comes to voltage headroom can be seen.

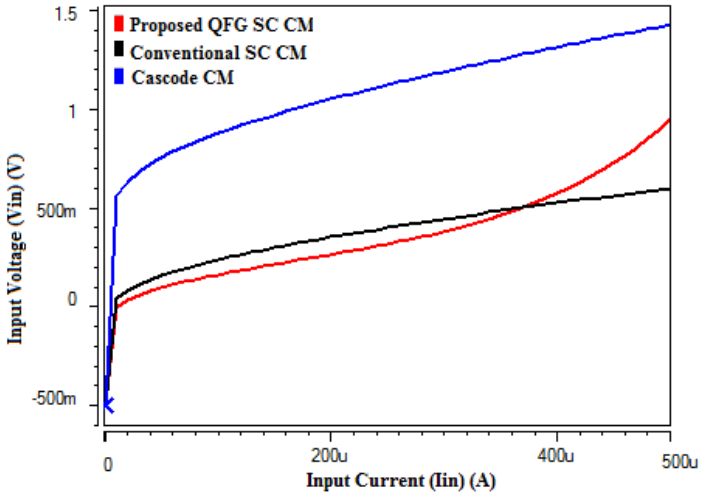


Figure 9: Input characteristics

The input and output resistance plots are shown in Figure 10 and Figure 11 respectively. Compared to conventional SC based CM, the proposed QFG-SC based CM input resistance becomes independent of $(1/g_{m1})$ which results in reduced resistance to $940\,\Omega$ from $1.6K\Omega$. The lowest input resistance is exhibited by the proposed QFG-SC CM. Similarly, comparing the output resistance in relation to the conventional cascode it gets increased by $(g_{m2}r_{04})$ times due to which the resistance is increased to $170K\,\Omega$ from $50K\,\Omega$. However, the output resistance is approximately equal to that of cascode. The frequency response is shown in Figure 12 where no bandwidth degradation is observed. The complete simulated Spice result is shown in tabulated form in Table 2.

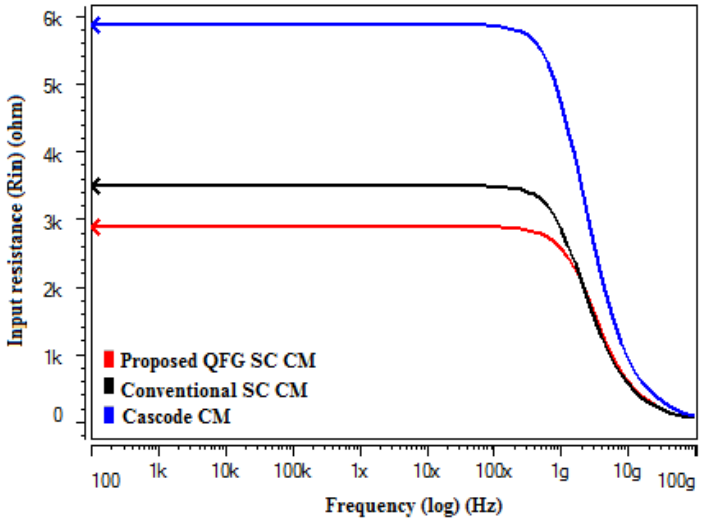


Figure 10: Input resistances

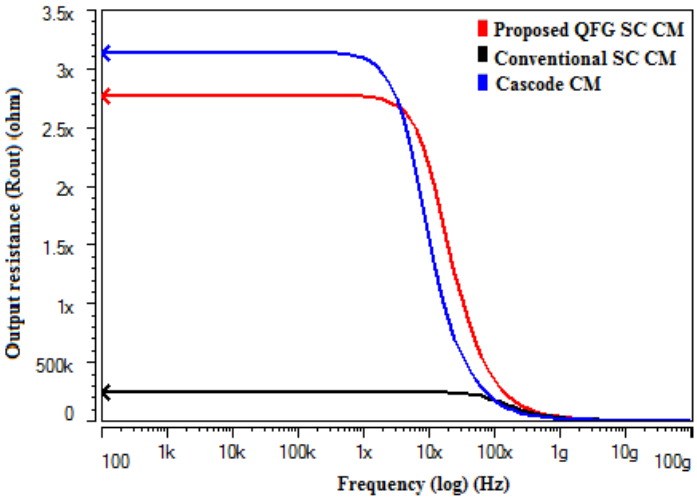


Figure 11: Output resistances

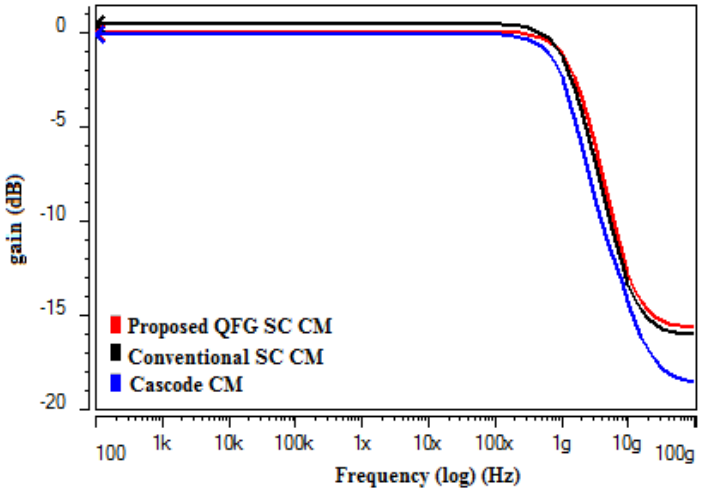


Figure 12: Frequency response

Parameters	Cascode CM	Conventional SC CM	Proposed QFG SC CM (Proposed)
Input current range (μA)	0-500	0-500	0-500
Input resistance (ohm)	5.87K	3.49K	2.88K
Output resistance (ohm)	3.14M	244K	2.77M
Bandwidth (Hz)	1.23G	1.52G	1.93G
Voltage Supply	±0.5V	±0.5V	±0.5V

Table 2: Performance analysis of Current Mirror

5. Conclusion

In this paper, a high performance design of self cascode structure has been presented. The improvement achieved is in terms of transconductance that has been possible due to change in the transistor mode of operation, possible by using the QFG technique. Further, the proposed QFG-SC structure is used in current mirror realizations which improved the parameters in terms of input and output resistances without affecting the bandwidth response. The performances achieved encourages its application in low power design.

References

Aggarwal, B., M. Gupta, and A. K. Gupta. 2013. "Analysis of low voltage bulk-driven self-biased high swing cascode current mirror". *Microelectronics Journal* 44, no. 3 (march): 225-35. https://doi.org/10.1016/j.mejo.2012.12.006.

Baek, K.-J., K.-Y. Na, and Y.-S. Kim. 2016. "Self-cascode structures using optional devices in standard CMOS technology". *IDEC Journal of Integrated Circuits and Systems* 2, no. 1 (april): 1-7.

Baek, K. -J., J.-M. Gim, H.-S. Kim, K.-Y. Na, N.-S. Kim, and Y.-S. Kim. 2013. "Analogue circuit design methodology using self-cascode structures". *Electronics Letters* 49, no. 9 (april): 591-92. https://doi.org/10.1049/el.2013.0554.

Bchir, M., I. Aloui, and N. Hassen. 2020. "A bulk-driven quasi-floating gate FVF current mirror for low voltage, low power applications". *Integration* 74 (september): 45-54. https://doi.org/10.1016/j.vlsi.2020.04.002.

Blalock, B. J., P. E. Allen, and G. A. Rincon-Mora. 1998. "Designing 1-V op amps using standard digital CMOS technology". *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 45, no. 7 (july): 769-80. https://doi.org/10.1109/82.700924.

Esparza-Alfaro, F., A. J. Lopez-Martin, R. G. Carvajal, and J. Ramirez-Angulo. 2014. "Highly linear micropower class AB current mirrors using Quasi-Floating Gate transistors". *Microelectronics Journal* 45, no. 10 (october): 1261-67. https://doi.org/10.1016/j.mejo.2014.02.006.

Esparza-Alfaro, F., A. J. Lopez-Martin, J. Ramírez-Angulo, and R. G. Carvajal. 2012. "Low-voltage highly-linear class AB current mirror with dynamic cascode biasing". *Electronics Letters* 48, no. 21 (october): 1336-38. https://doi.org/10.1049/el.2012.3081.

Fujimori, I., and T. Sugimoto. 1998. "A 1.5 V, 4.1 mW dual-channel audio delta-sigma D/A converter". *IEEE Journal of Solid-State Circuits* 33, no. 12 (december): 1863-70. https://doi.org/10.1109/4.735525.

Galup-Montoro, C., M. C. Schneider, and I. J. B. Loss. 1994. "Series-parallel association of FET's for high gain and high frequency applications". *IEEE Journal of Solid-State Circuits* 29, no. 9 (september): 1094-101. https://doi.org/10.1109/4.309905.

Gerosa, A., and A. Neviani. 2003. "Enhancing output voltage swing in low-voltage micro-power OTA using self-cascode". *Electronics Letters* 39, no. 8 (april): 638-39. https://doi.org/10.1049/el:20030436.

Hasler, P., and T. S. Lande. 2001. "Overview of floating-gate devices, circuits, and systems". *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 48, no. 1 (january): 1-3. https://doi.org/10.1109/tcsii.2001.913180.

Khateb, F. 2014. "Bulk-driven floating-gate and bulk-driven quasi-floating-gate techniques for low-voltage low-power analog circuits design". *AEU - International Journal of Electronics and Communications* 68, no. 1 (january): 64-72. https://doi.org/10.1016/j.aeue.2013.08.019.

———. 2015. "The experimental results of the bulk-driven quasi-floating-gate MOS transistor". *AEU - International Journal of Electronics and Communications* 69, no. 1 (january): 462-66. https://doi.org/10.1016/j.aeue.2014.10.016.

Lopez-Martin, A. J., J. Ramírez-Angulo, R. G. Carvajal, and J. M. Algueta. 2008. "Compact class AB CMOS current mirror". *Electronics Letters* 44, no. 23 (november): 1335-36. https://doi.org/10.1049/el:20082419.

Manhas, P. S., S. Sharma, K. Pal, L. K. Mangotra, and K. K. S. Jamwal. 2008. "High performance FGMOS-based low voltage current mirror". *Indian Journal of Pure and Applied Physics* 46, no. 5: 355-58.

Na, K.-Y., K.-J. Baek, and Y.-S. Kim. 2012. "N-channel dual-workfunction-gate MOSFET for analog circuit applications". *IEEE Transactions on Electron Devices* 59, no. 12 (december): 3273-79. https://doi.org/10.1109/ted.2012.2219865.

Raj, N., A. K. Singh, and A. K. Gupta. 2014a. "Low power high output impedance high bandwidth QFGMOS current mirror". *Microelectronics Journal* 45, no. 8 (august): 1132-42. https://doi.org/10.1016/j.mejo.2014.05.005.

———. 2014b. "Low-voltage bulk-driven self-biased cascode current mirror with bandwidth enhancement". *Electronics Letters* 50, no. 1 (january): 23-25. https://doi.org/10.1049/el.2013.3600.

———. 2016a. "High performance current mirrors using quasi-floating bulk". *Microelectronics Journal* 52 (june): 11-22. https://doi.org/10.1016/j.mejo.2016.02.012.

———. 2016b. "Low voltage high performance bulk driven quasi-floating gate based self-biased cascode current mirror". *Microelectronics Journal* 52 (june): 124-33. https://doi.org/10.1016/j.mejo.2016.04.001.

———. 2016c. "Low voltage high output impedance bulk-driven quasi-floating gate self-biased high-swing cascode current mirror". *Circuits, Systems, and Signal Processing* 35, no. 8 (august): 2683-703. https://doi.org/10.1007/s00034-015-0184-4.

———. 2017. "Low voltage high bandwidth self-biased high swing cascode current mirror". *Indian Journal of Pure and Applied Physics* 55, no. 4 (april): 245-53.

Rajput, S. S., and S. S. Jamuar. 2001. "Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications". *IEE Proceedings - Circuits, Devices and Systems* 148, no. 5 (october): 273-78. https://doi.org/10.1049/ip-cds:20010441.

Ramirez-Angulo, J., A. J. Lopez-Martin, R. G. Carvajal, and F. M. Chavero. 2004. "Very low-voltage analog signal processing based on quasi-floating gate transistors". *IEEE Journal of Solid-State Circuits* 39, no. 3 (march): 434-42. https://doi.org/10.1109/jssc.2003.822782.

Ramirez-Angulo, J., C. A. Urquidi, R. Gonzalez-Carvajal, A. Torralba, and A. Lopez-Martin. 2003. "A new family of very low-voltage analog circuits based on quasi-floating-gate transistors". *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 50, no. 5 (may): 214-20. https://doi.org/10.1109/tcsii.2003.811434.

Sharma, S., S. S. Rajput, L. K. Mangotra, and S. S. Jamuar. 2006. "FGMOS current mirror: Behaviour and bandwidth enhancement". *Analog Integrated Circuits and Signal Processing* 46, no. 3 (march): 281-86. https://doi.org/10.1007/s10470-006-1625-6.

Zhang, X., and E. I. El-Masry. 2004. "A regulated body-driven CMOS current mirror for low-voltage applications". *IEEE Transactions on Circuits and Systems II: Express Briefs* 51, no. 10 (october): 571-77. https://doi.org/10.1109/tcsii.2004.834536.