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Comparative Study of Multilevel Converters using DQ Current Control

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Abstract

This paper presents a comprehensive comparative analysis of different multilevel converter topologies, including 2-level, Neutral Point-Clamped (NPC), Cascaded H-Bridge (CHB), and T-Type converters using the DQ current control strategy. The study aims to evaluate the performance of these topologies concerning current Total Harmonic Distortion (THD) and ripple in the direct and quadrature components of the current.

A mathematical model of the grid is presented to facilitate the simulation study. The DQ current control scheme is implemented to regulate the current in both the direct and quadrature axes. The simulations are conducted under various operating conditions to capture the converters' performance across different load scenarios and modulation techniques.

Results indicate significant variations in the performance metrics among the different converter topologies. The 2-level converter exhibits higher THD and ripple compared to the more complex multilevel topologies.

1. Introduction

In power electronics, the quest for efficient, high-performance, and reliable energy conversion solutions has driven continuous innovation. Multilevel converters have emerged as a cornerstone technology in this pursuit, offering transformative advantages in various applications, including renewable energy integration, electric vehicles, and industrial drives.

Multilevel converters have emerged as a solution that offers several technical advantages over conventional topologies (Rodriguez et al. 2009).

This type of converters are currently considered as one of the industrial solutions for high dynamic performance and power quality demanding applications, covering a power range from 1 to 30MW (Rodriguez et al. 2009). Among the reasons for their success are: higher voltage operating capability, lower common-mode voltages, reduced voltage derivatives (dv/dt), voltages with reduced harmonic contents, near sinusoidal currents, smaller input and output filters (if necessary), increased efficiency, and in some cases possible fault tolerant operation (Barros, Martins, and Pinto 2022; Komurcugil and Bayhan 2021; Schweizer and Kolar 2013; Potty et al. 2020).

They have several applications, such as integrating distributed generation, electric vehicles, and motor drives. Multilevel converters represent a paradigm shift in power electronics, departing from the traditional two-level voltage-source converters (Kouro et al. 2018).

Multilevel converters are power conversion systems composed of an array of power semiconductors and capacitive voltage sources that, when properly connected and controlled, can generate a multiple step voltage waveform with variable and controllable frequency, phase and amplitude (Franquelo et al. 2008). To be called a multilevel converter, each phase of the converter has to generate at least three different voltage levels. This differentiates the classic two-level voltage source converter (2L-VSC) from the multilevel family.

As shown in **Figure 1** they are classified as voltage source converters that allow to reach voltage operation values above the limits imposed by

semiconductor technology (Kouro et al. 2018).

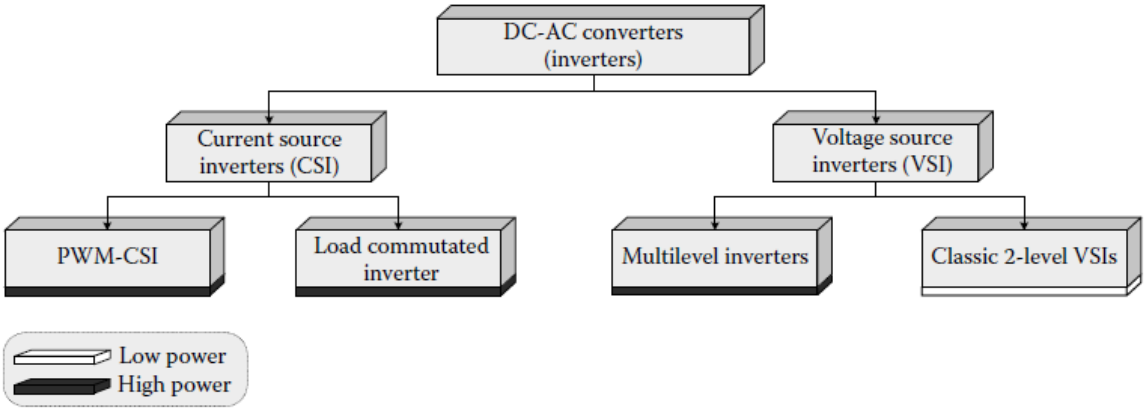


Figure 1: Multilevel Converters Classification in the DC-AC Converters (Kouro et al. 2018).

There are a large number of multilevel converter topologies reported in the literature, but the most common multilevel converter topologies in industry are diode-clamped converters, also called Neutral Point-Clamped (NPC) converters, Active-NPC, T-Type, CHB converters, and FC converters (Hasan et al. 2017; Schweizer and Kolar 2013; Pan et al. 2019). Some new topologies are derived from the classic ones, such as modular solutions where the matrix multilevel converter can be highlighted (Wang et al. 2020; Priya et al. 2019).

Modulation techniques for multilevel converters can be divided into two main groups: techniques based on the space vector concept and techniques based on voltage levels. For high switching frequency, the multicarrier Pulse-Width Modulation (PWM) and Space Vector Modulation (SVM) are the most adequate, and for low switching frequency, nearest level control is a suitable option (Kouro et al. 2018; Komurcugil and Bayhan 2021).

Currently, this class of converters has attracted even more interest from researchers and industry due to the emergence of more efficient semiconductors devices designated as Wide Band Gap Semiconductors. With this type of semiconductors, it is possible to design converters with a higher gravimetric (kW/Kg) and volumetric (KW/L) power density, allowing, for example, the deployment of more efficient and compact electric vehicle charging stations.

This paper will explore the main multilevel topologies and modulation techniques. Using PLECS, which is a simulation platform, the VSC 2-level converter, the NPC, the CHB and T-type will be implemented, as well as the appropriate modulation techniques. In this way, it will be possible to compare the performance of multilevel topologies in comparison with a 2-level topology. In addition, DQ current control is implemented. This control technique allows constant reference values to be used to control the voltage at the converter terminals, the value of the direct(i_d) and quadrature(i_q) components of current and active and reactive power.

This paper is organized as follows:

Section 2 presents the methodology of the work to be carried out. Section 3 presents and discusses the results obtained from the different simulations. In 4, final considerations are made, and future work is identified.

2. Methodology

In this section, the electrical model and the control method of the three-phase voltage source converters are presented. Reference transformation used for the converter control is described. Finally, a full characterization of the control scheme in continuous and discrete time of the converter is provided.

2.1. System Presentation

This work studies the control of multilevel converters connected to the power grid. The proposed system consists of a balanced sinusoidal source(v_{abc}), an RL filter and a voltage source converter.

The proposed system is shown in **Figure 2**, and its dynamics are given by equation (1).

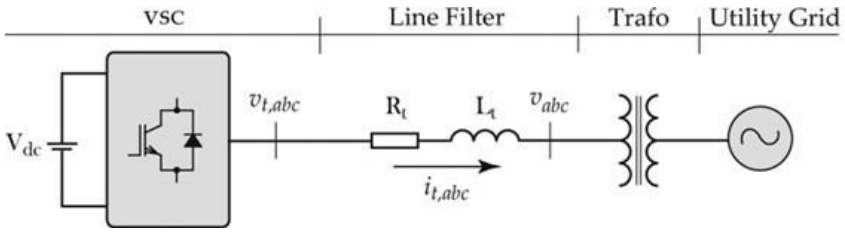


Figure 2: Power Circuit Schematic (Bahrani et al. 2013).

$$v_{t,abc} = R_t i_{t,abc} + L_t \frac{di_{t,abc}}{dt} + v_{abc} \quad (1)$$

where $v_{t,abc}$ and v_{abc} are the voltage at the VSC terminals and the grid voltage in abc frame, respectively.

The main parameters of the system are presented in **Table 1**.

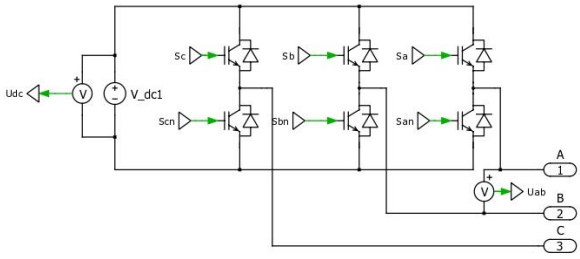
Parameters	Symbol	Value	Unit
Nominal Voltage L-L	V_{rms}	400	V
Nominal Frequency	f	50	Hz
Line Resistor	R	0.15	Ω
Inductance	L	5e-3	H
Nominal DC Voltage	V_{DC}	800	V

Table 1: System Parameters.

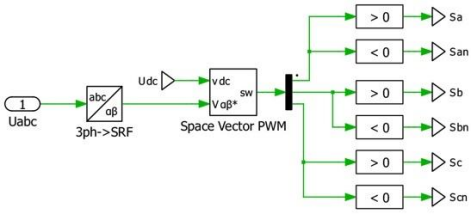
2.2. Voltage Source Converters and Modulation

In order to study the main VSC topologies, the following were selected: 2 level, 3 level NPC, 3-level NPC and 5 level CHB. The aim is to implement modulation and control techniques to study the converters' response.

As shown in the **Figure 3**, **Figure 4** ,**Figure 5Figure 6** and the modulation techniques for 2-level, 3-level NPC , 3-level T-type and 5-level CHB were as follows: SVM, phase-disposition PWM(2x) and phase-shift PWM, respectively.

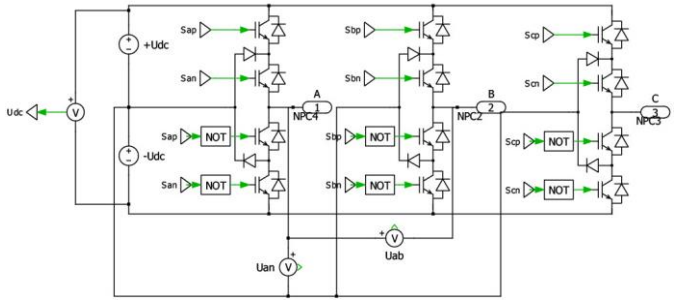


(a) Schematic

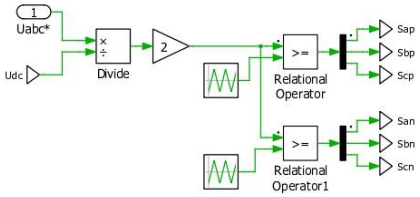


(b) Modulation: SVM

Figure 3: 2-Level VSC



(a) Schematic

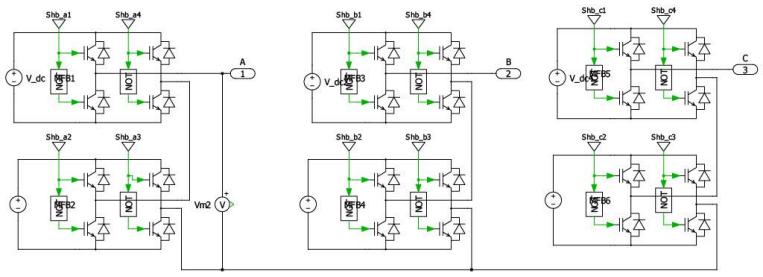


(b) Modulation: PD-PWM

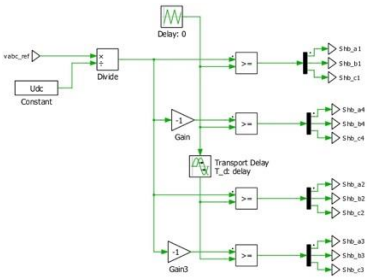
Figure 4: 3-Level NPC

2.3. Voltage Oriented Control

The converter's control scheme generates the modulator signals from current reference values. The decoupled DQ-current controller described in (Bahrani, Kenzelmann, and Rufer 2011; Bahrani et al. 2013; Tahir et al. 2018) was implemented for the proposed work. **Figure 7** presents the control scheme adopted.

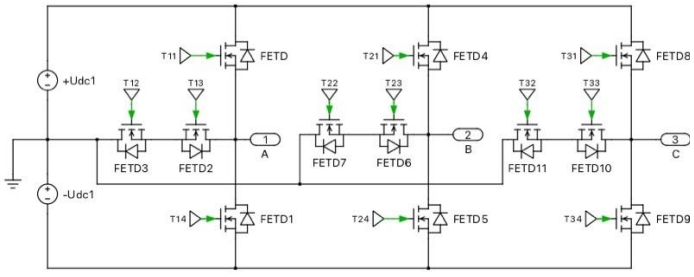


(a) Schematic.

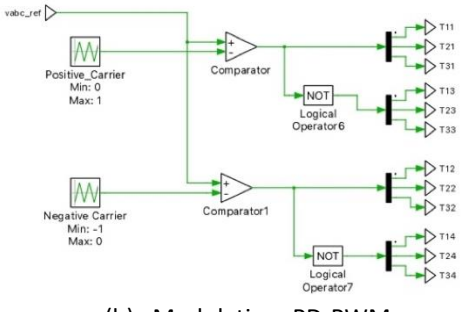


(b) Modulation: PS-PWM

Figure 5: CHB Converter.



(a) Schematic.



(b) Modulation: PD-PWM

Figure 6: T-Type Converter.

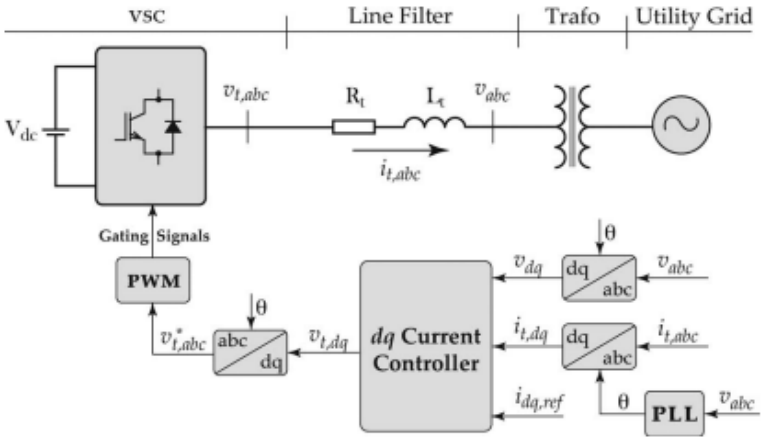


Figure 7: Power Circuit and Control Schematic (Bahrani et al. 2013).

PI controllers are commonly used in control schemes for VSC to track constant DC commands. However, they are inadequate for sinusoidal voltage or current references. To simplify the analysis and control, the two-dimensional frames, the αβ frame, obtained using Clarke transform, and the DQ frame, obtained using Park Transform, are used. The αβ frame simplifies the problem of controlling three sinusoids to two equivalent sinusoids. The dq frame simplifies the problem by transforming the previous two sinusoid signal into two DC commands and provides several benefits, such as:

- Computation in dq frame is significantly easier;
- It allows for system decoupling control of the active and reactive components of the currents;
- PI controllers can be used since they are effective and reliable when the quantities are DC nature.

The first step is transforming equation (1 to αβ frame. This results in the transition from an abc frame to a Stationary Reference Frame (SRF) with two variables $\alpha \; and \; \beta$. Since α and β are orthogonal components, the variables in this frame can be treated as complex numbers. Thus, the following equation is obtained:

$$v_{t,\alpha\beta0} = R_t i_{t,\alpha\beta0} + L_t \frac{di_{t,\alpha\beta0}}{dt} + v_{\alpha\beta0} \tag{2}$$

Next, the αβ-to-dq transformation $u_{dq0} = u_{\alpha\beta0} e^{-j\omega t}$ is applied equation (2) and the SRF is transformed into a Rotating Reference Frame (RRF). The grid angle ϕ is obtained from the alpha and beta components of the grid voltage using the 2-argument arctangent or $atan2$: $\phi = atan2\left(\frac{v_\beta}{v_\alpha}\right)$. A Phase Lock Loop(PLL) can also be used to extract the grid angle position. Equation 3 describes the VSC ac side variables in the dq-frame.

$$v_{t,dq} = R_t i_{dq} + L_t \frac{di_{t,dq}}{dt} + j\omega L_t i_{t,dq} + v_{dq} \tag{3}$$

Separating the real and imaginary terms, the dynamics of the d and q axis are deduced:

$$R_t i_{t,d} + L_t \frac{di_{t,d}}{dt} = v_{t,d} + \omega L_t i_{t,q} - v_d \tag{4}$$

$$R_t i_{t,q} + L_t \frac{di_{t,q}}{dt} = v_{t,q} - \omega L_t i_{t,d} - v_q \tag{5}$$

To control the $i_{t,d}$ and $i_{t,q}$ components, it is necessary to obtain the references of the voltage values at the VSC terminals. By simplifying the equations (4 and (5 where v_d and v_q correspond to the dq components of the grid voltage, and $\omega L_t i_{t,q}$ and $-\omega L_t i_{t,d}$ correspond to the coupling terms, the references $v_{t,d}$ and $v_{t,q}$ are obtained:

$$v_{t,d} = u_{c,d} - \omega L_t i_{t,q} + v_d \tag{6}$$

$$v_{t,q} = u_{c,q} + \omega L_t i_{t,d} + v_q \tag{7}$$

where $u_{c,d}$ and $u_{c,q}$ are the control signals for the d and q axes respectively and equal to:

$$u_{c,d} = R_t i_{t,d} + L_t \frac{di_{t,d}}{dt} \tag{8}$$

$$u_{c,q} = R_t i_{t,q} + L_t \frac{di_{t,q}}{dt} \tag{9}$$

Applying the Laplace transform, we obtain the transfer function of the decoupled system, as shown:

$$G(s) = \frac{1/R_t}{1 + (L_t/R_t)s} = \frac{K_s}{1 + T_s s} \tag{10}$$

The values $K_s = 1/R_t$ and $Ts = R_t/L_t$ correspond to the proportional gain and time constant(T_i) of the PI controller, respectively.
The reference values $v_{t,d}$ and $v_{t,q}$ are then applied to the inverse Park transform to obtain the references $v_{t,\alpha}$ and $v_{t,\beta}$ in the rotational reference. The angle ϕ, in radians, is used in this transformation. Finally, the inverse Park transform is applied to obtain the reference values V_{abc}^{ref} in the abc reference frame. As explained above, the V_{abc}^{ref} is used to obtain the modulation signal, $v_{modulator}$.

$$v_{modulator} = \frac{V_{abc}^{ref}}{V_{DC}/2} \tag{11}$$

2.4. Simulation in PLECS

The power system, modulation and control techniques were implemented in PLECS software. The controller described above was built using software blocks, obtaining the model in continuous time. However, with the objective of implementing the system in the laboratory in a future project, discrete-time control was also developed.

Figure 8 shows the continuous time dq current controller implemented in PLECS.

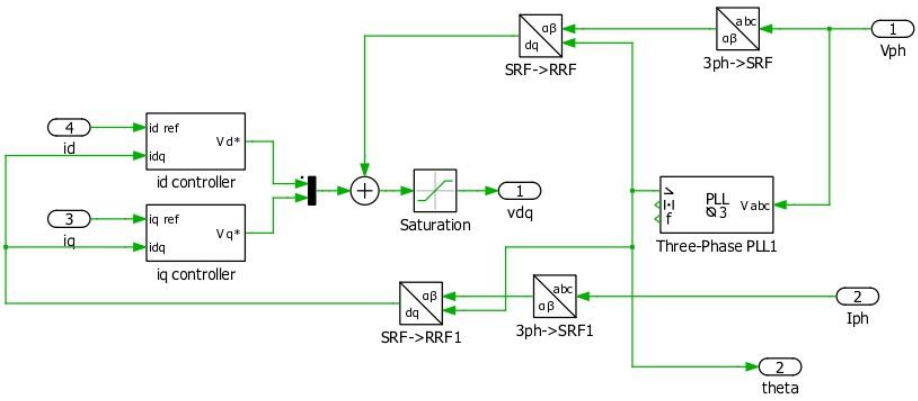


Figure 8: DQ Current Controller implemented in PLECS.

To obtain the discrete-time PI controller, the bilinear transform or Tustin method shown in equation 12 was used, where Ts corresponds to the sampling time.

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{12}$$

By substituting s in the transfer function of the PI controller in the frequency domain, as given in equation 13, with equation 12 representing the transfer function of the PI controller in the Z domain, we derive equation 14.

$$U(s) = k_p\left(E(s) + \frac{1}{T_i}\frac{1}{s}E(s)\right) \tag{13}$$

$$U(z) = z^{-1}U(z) + k_p\big(E(z) - z^{-1}E(z)\big) + \frac{k_p}{T_i}\frac{T_s}{2}\big(E(z) + z^{-1}E(z)\big) \tag{14}$$

Considering that z^{-1} indicates the preceding value within a specific interval of the z domain, we can express equation 14 as equation 15. In this equation $u(n)$ and $e(n)$ represent the current output and error, while $u(n-1)$ and $e(n-1)$ express the output value and error from the previous iteration. The constants k_p , T_i and T_s correspond respectively to the proportional gain, integral time and sampling time.

$$u(n) = u(n-1) + k_p\big(e(n) - e(n-1)\big) + \frac{k_p}{Ti}\frac{T_s}{2}\big(e(n) + e(n-1)\big) \tag{15}$$

3. Results and Discussion

This section presents and discusses the simulation and the results for the four VSC in continuous and discrete time.

3.1. Simulation Description

In order to simulate the converter's operation, specific operating conditions were defined. Thus, although it is possible to define various combinations of operating points, for this work the operation of the converter as an inverter is studied. The i_d and i_q currents were set for the converter to function as an inverter, allowing the system's response to steps ($R(s) = 1/s$) to be studied.

Figure 9 shows the values of active and reactive power supplied to the grid and calculated from equation 16 and 17.

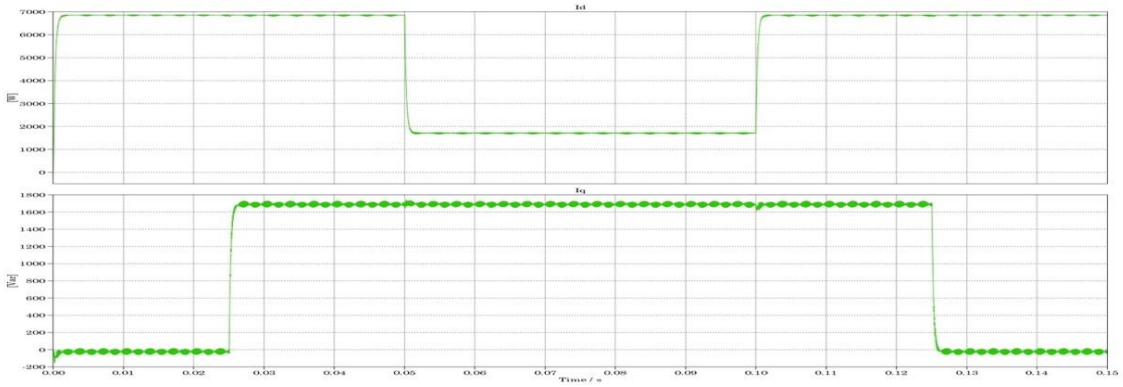


Figure 9: Active and Reactive Power at the grid.

$$P = \frac{2}{3}\left(v_d * I_d + vq * I_q\right) \tag{16}$$

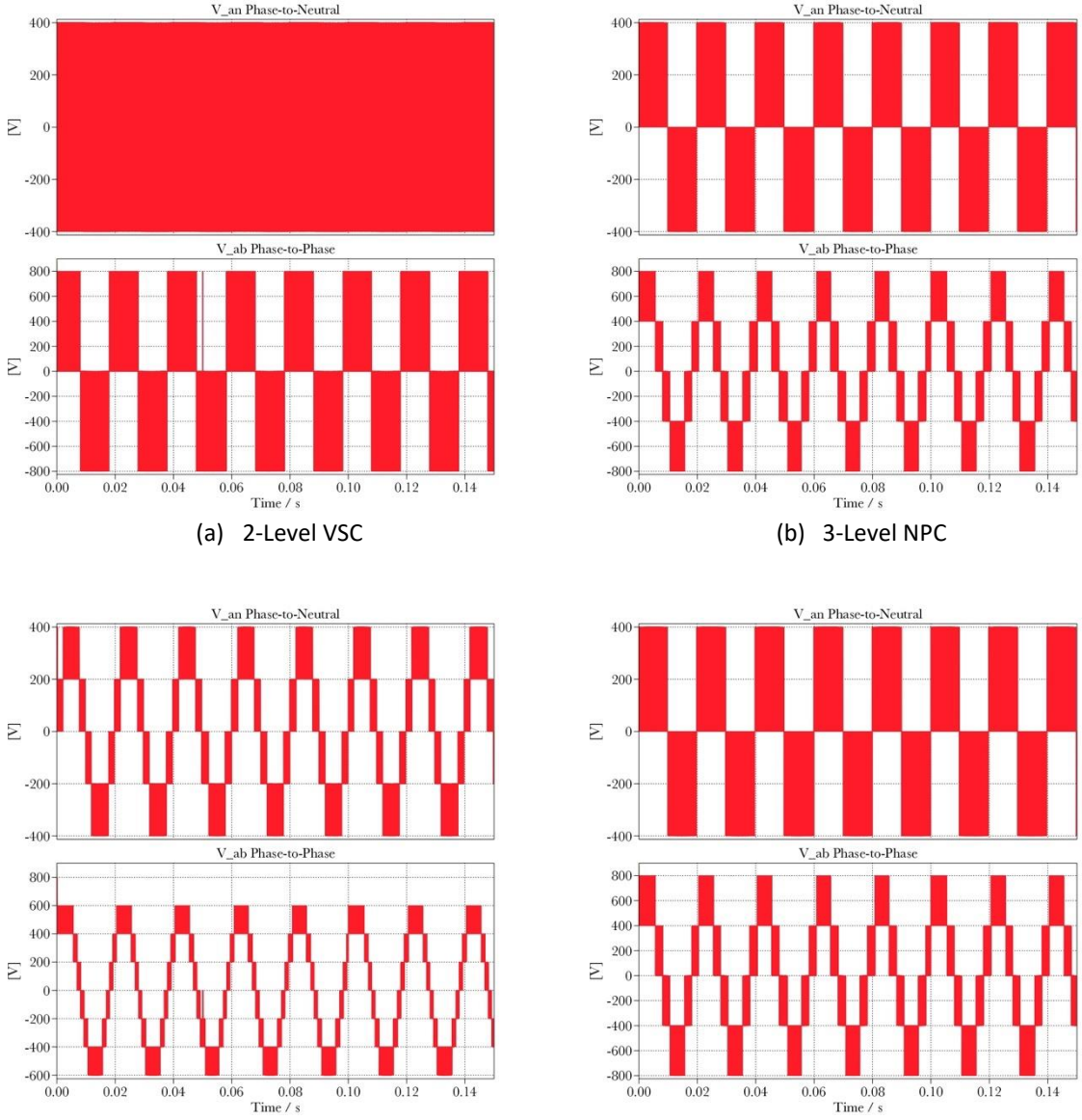
$$Q = \frac{2}{3}\left(v_d * I_q - vq * I_d\right) \tag{17}$$

The converter's operating periods are highlighted:

- $[0{,}0.025]$s: active and reactive power of 7kW(id=20A) and 0 VAr(iq=0A);
- $[0.0250.05]$s: active and reactive power of 7kW(id=20A) and 1750 VAr(iq=5A);
- $[0.050.1]$s: active and reactive power of 1750kW(id=5A) and 1750 VAr(iq=5A);
- $[0.10.125]$s: active and reactive power of 7kW(id=20A) and 1750 VAr(iq=5A);
- $[0.1250.15]$s: active and reactive power of 7kW(id=20A) and 0 VAr(iq=0A);

The values of proportional gain and integrative time that were defined in the previous chapter were adjusted to obtain a better response. Thus, the values of k_p and T_i used in the simulations were 20 and 0.001 s, respectively.

In **Figure 10** the voltages at the terminal of the converters are presented.



(a) 2-Level VSC (b) 3-Level NPC

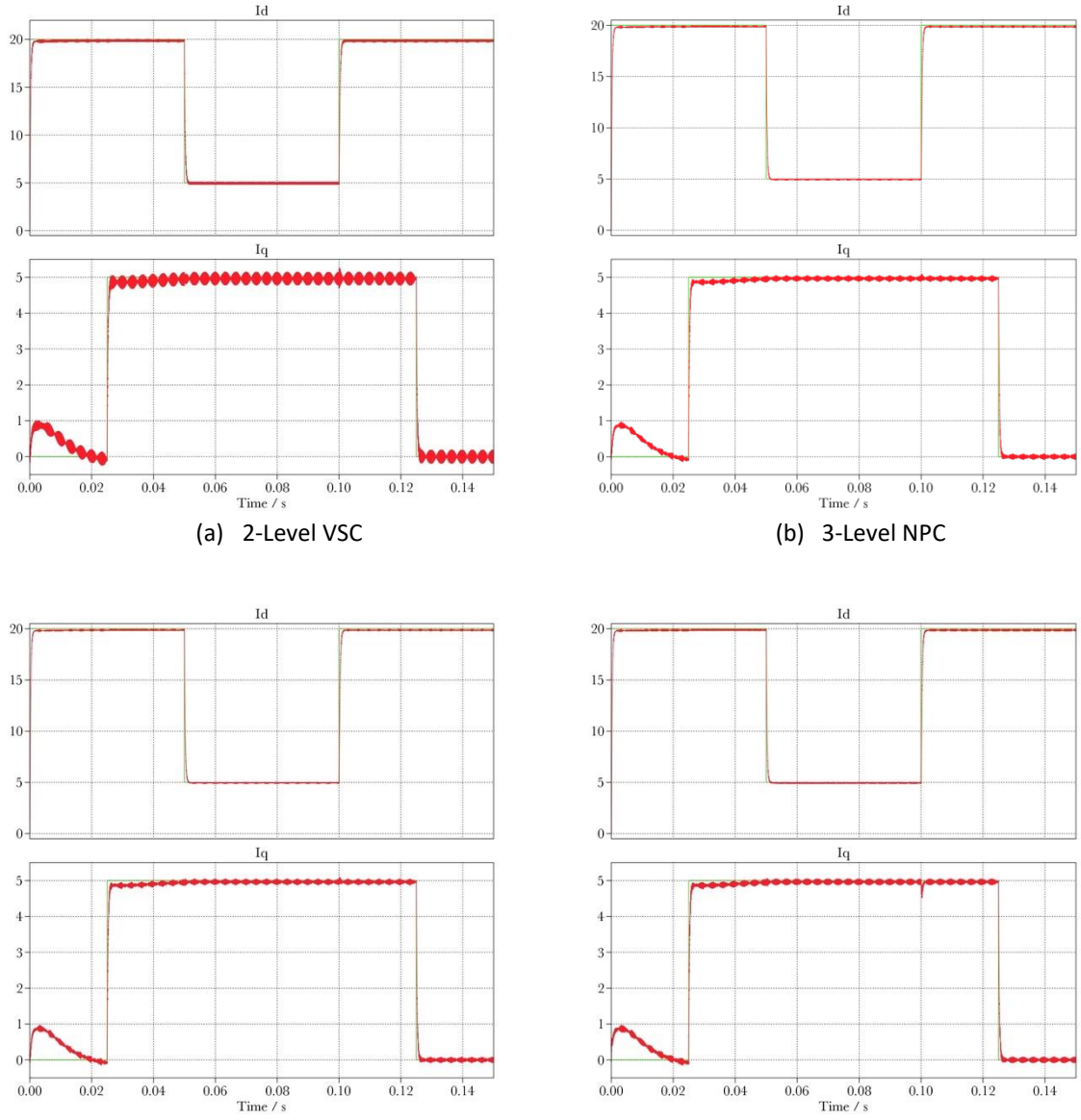
(c) 5-Level CHB (d) 3-Level T-Type

Figure 10: Terminal Voltages.

3.2. Results Continous Time

The continuous-time simulation produced the results shown in **Figure 11** regarding the four converters. These graphs show the direct and quadrature components of the current.

When comparing the reference currents with the results obtained, it can be seen that the controller works according to the model presented in the previous section. However, the change of reference on the d-axis causes a small disturbance in the q component (and vice versa). Therefore, the axes are not completely decoupled.



(a) 2-Level VSC (b) 3-Level NPC

(c) 5-Level CHB (d) 3-Level T-Type

Figure 11: Simulation Results: Continuous Time

Table 2 shows some parameters relating to the current in the abc reference, the Total Harmonic Distortion (THD), and in the dq reference, the ripple and the steady-state error. The THD was measured during the period $[0.1250.15]$, where the direct and quadrature currents were equal to 20 A and 5 A, respectively.

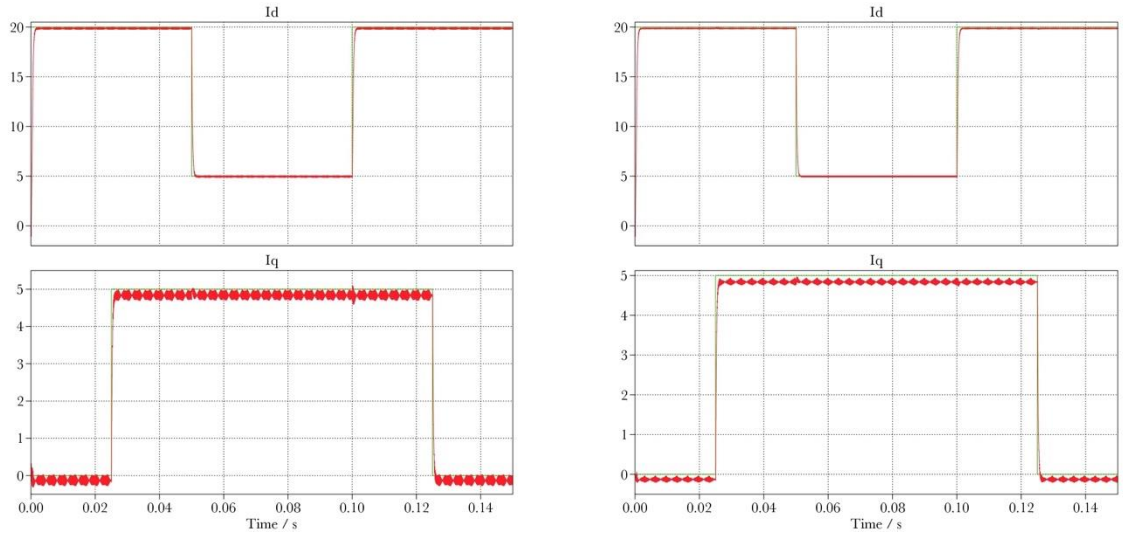
VSC	THD(%)	$\Delta i_d \left(i_{d_{ref}} = 20A\right)$	$\Delta i_q \left(i_{q_{ref}} = 5A\right)$	S.S. Error $i_{dq_{ref}} - i_{dq}$
2-level	$137.49 * 10^{-4}$	0.1905 A	0.3709 A	0.1489
3-level NPC	$72.53 * 10^{-4}$	0.1268 A	0.1724 A	0.1488
5-Level CHB	$58.35 * 10^{-4}$	0.1006 A	0.1104 A	0.1488
3-Level T-Type	$78.23 * 10^{-4}$	0.1315 A	0.1716 A	0.1489

Table 2: Results Continuous Time: Current Parameters

From the analysis of the results in the table, the converter with the best harmonic performance is CHB, as it generates a voltage waveform with 5 levels between phases. As expected, the 2-level converter has the highest THD value. The CHB presents the lowest ripple values in the i_d and i_q currents and steady-state error, followed by the NPC converter. The settling time of the i_d and i_q currents, of the four converters is approximately 1 ms.

3.3. Results Discrete Time

The results obtained from the discrete-time simulation are shown in **Figure 12**. The switching frequency was kept at 20 kHz, and the sampling time is $20\mu s$(60 kHz) . The constants k_p and T_i are the same as for the continuous-time controller. **Table 3** shows the parameters under analysis concerning the currents of the grid.



(a) 2-Level VSC (b) 3-Level NPC

(c) 5-Level CHB (d) 3-Level T-Type

Figure 12: Simulation Results: Discrete Time

As in the continuous-time simulation, the controller follows the imposed i_d and i_q references. The CHB converter has the lowest THD value and the lowest ripple and error values in the

steady state. It can again be seen that changing one of the dq references affects the other, with an increase in ripple in the transient period.

VSC	THD(%)	$\Delta i_d \left(i_{d_{ref}} = 20A\right)$	$\Delta i_q \left(i_{q_{ref}} = 5A\right)$	S.S. Error $i_{dq_{ref}} - i_{dq}$
2-level	$132.43 * 10^{-4}$	0.2070 A	0.2893 A	0.1489
3-level NPC	$72.53 * 10^{-4}$	0.1099 A	0.1770 A	0.1488
5-Level CHB	$58.35 * 10^{-4}$	0.0876 A	0.0979 A	0.1363
3-Level T-Type	$78.23 * 10^{-4}$	0.1259 A	0.1837 A	0.1355

Table 3: Results Simulation in Discrete Time

4. Conclusions

From the review of the state of the art of multilevel converters, it is clear that the NPC, FC and CHB topologies are the most studied and have the greatest number of applications. Although the 2-level converter is simpler to build and cheaper, in applications where the voltage levels exceed the limit of the semiconductors or the high efficiency of the converter is a requirement, multilevel converters are the ideal solution. The NPC converter allows half of the DC voltage to be distributed among the 4 semiconductors per-phase and is used in medium-power applications. The CHB converter stands out for its modularity, scalability, and excellent harmonic performance.

The PS-PWM, PD-PWM and SVM modulation techniques are the most widely used. PS-PWM and PD-PWM are techniques based on reference voltage values as a function of time. SVM is a technique based on the representation of the voltage vector in the stationary reference frame.

The simulation developed in software validated the theoretical study, in which multilevel converters show better results than 2-level VSC in terms of output signal quality, namely ripple and THD. The CHB converter stood out among the four converters implemented for having the lowest THD value.

The DQ decoupled current controller did not make it possible to achieve zero error in steady-state and total decoupling of the axes. Although its advantage is that it decouples the active and reactive power components and makes control simpler, some improvements still need to be made and the proportional gain and integrative time constant need to be adjusted.

Simulation in continuous time and discrete time showed similar results, although ripple and THD decreased in the discrete-time simulation.

As future work, the following is identified: eliminate the non-zero error in the steady state of the controller, improve the discrete controller, implement the modulation of the converter in C code, implement and validate the controller using a laboratory prototype.

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